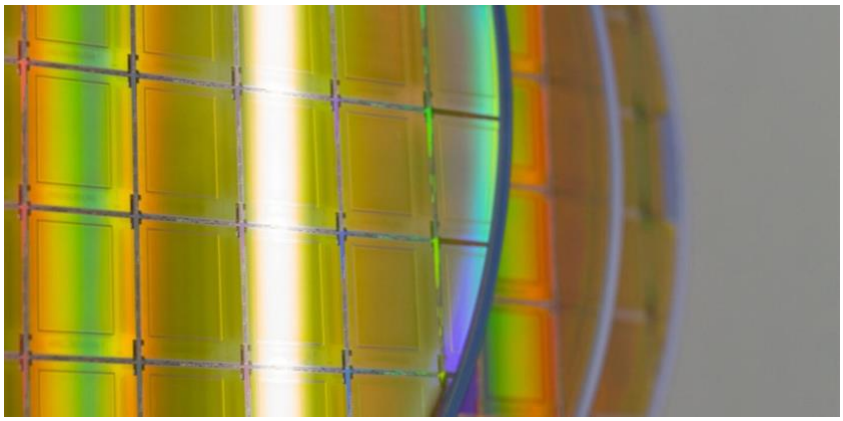
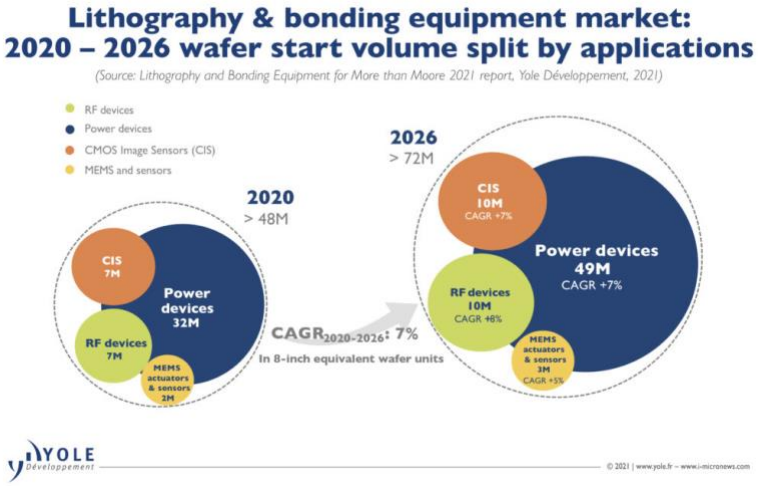
Lithography and bonding equipment drives More-than-Moore technology innovation – An interview with EV Group and Yole Développement – January 13, 2022



The More-than-Moore (MtM) concept covers a large range of devices such as MEMS and sensors, RF, power, CIS, as well as their integration with logic and memory in Advanced Packaging. The MtM philosophy is to increase the performance of electronics systems by integrating new functionalities. Any equipment capable of manufacturing such devices and integrated systems has to be either dedicated for a precise process or be flexible enough to handle various processes and substrates. Thus, capital investment needs to be made by manufacturers specifically for MtM-dedicated equipment, and for lithography and bonding technologies, this investment is expected to have a CAGR exceeding 9% and 7%, respectively, in the coming five years.



The current increases in revenue and advances in equipment adaptation for MtM devices have been thoroughly reviewed in the technology & market report **Bonding and Lithography Equipment for More-than-Moore devices**, published recently by **Yole Développement (Yole).** Among the featured equipment

manufacturers, **EV Group** is one of the leading equipment providers for lithography as well as permanent and temporary bonding in the MtM space. EV Group works in close collaboration with industry leaders to leverage MtM technical challenges and create new business opportunities.

Thomas Uhrmann, PhD, Head of Business Development at EV Group, and Jean-Christophe Eloy, President & CEO of Yole, had the opportunity to debate about the evolution of the industry and review the roadmap dedicated to equipment for MtM device fabrication.

The interview presented below was moderated by **Taguhi Yeghoyan, PhD, Semiconductor Manufacturing Technology and Market Analyst at Yole.**

Taguhi Yeghoyan (TY): Please introduce EV Group and its history in shaping the MtM space and current interests?

Thomas Uhrmann (TU): For more than 15 years, we have been developing and revolutionizing bonding and lithography solutions for 3D and advanced packaging for MtM. One EV Group milestone was the development of fusion and hybrid bonding, which has evolved from an R&D application to an industry standard. The same is true for our temporary bonding and debonding, where we offer the most comprehensive portfolio on the market and continue to advance the technology. The current driver for MtM is the need for flexible solutions, as there are many different implementation options for how MtM can be achieved, whether in a more front-end of the line process or more traditional advanced packaging process. Closing this gap and establishing new, differentiated technologies and process solutions to drive MtM is our goal.

Megatrends are boosting the semiconductor industry and the development of the companies behind it. Despite the COVID-19 pandemic, 5G, AI, smart automotive and electrification, mobile, AR/VR, voice processing, and hyperscale datacenters all contribute to the growth of this sector…

TY: Could you explain to our readers the vision of Yole on these megatrends? How do they impact the semiconductor industry?

Jean-Christophe Eloy (JCE): These megatrends are pushing the industry in three main ways. Firstly, we're going to see much more semiconductor content in many different systems. Take mobile phones – even though the number of mobile phones being sold is not increasing, the value and number of semiconductors in the mobile phone is increasing, and we can say the same for other applications relating to the IoT, automotive, Industry 4.0, and other sectors. Ultimately, this growth in semiconductor content means we'll see more wafers being manufactured.

Secondly, these megatrends are bringing technology changes that will also drive growth. For example, 5G sees the industry transitioning from LDMOS semiconductors to devices based on, say, gallium nitride and silicon carbide. Also, data centers need to provide faster connectivity yet consume less power and are moving from copper interconnections to fiber optics. Such technology changes are driving investment, which, of course, will bring more industry growth.

Lastly, the megatrends are drawing new players into the market. Amazon, Google, Microsoft, and Apple employ huge teams to design the chips and devices they need for themselves. At the same time, automotive OEMs are also designing their own chips. We've just seen Ford sign Global Foundries to manufacture more chips for its own vehicles and other US auto-makers. All in all, the megatrends are driving growth and changing the structure of the entire semiconductor industry.

EV Group has traditionally been one of the leading equipment providers for front-end fabrication of MtM devices such as MEMS, CIS, or power. Moreover, advanced packaging has entered the MtM space for several years now.

TY: Could you please share your vision with i-Micronews readers on the following MtM aspects? In your opinion, which end-applications will lead the MtM device roadmap? What are the innovations in the MtM space, and what requirements do they have for manufacturing process flows?

TU: EVG is an innovator that has been working with industry leaders on 3D integration technologies for many years. Although many 3D concepts have been explored and developed over the years, scaling and mass production in monolithic 2D has been more cost-effective in most cases in the past. While More Moore will continue with certainty, 3D integration will nevertheless be essential in the future. On the one hand, advances in scaling will require 3D to handle interconnect density, signal bandwidth and signal

timing from a system perspective. On the other hand, several cost drivers are driving MtM applications. System complexity drives up the size of chips, increasing the risk of losing a chip with only a single defect and decreasing overall yield. The shift to smaller stacked chips is already providing a yield advantage. In the future, another yield driver in MtM will be to use devices from different sources and combine them in new systems. Future complexity will be in the design, system segmentation, and management of multiple wafer and chip sources. Overall, the trend toward higher interconnect density in MtM will continue, enabling chip segmentation at an earlier metal level and higher bandwidth interconnects. Today, we are at 20µm solder interconnects, though interconnect density will soon increase by a factor of 10 for leading MtM devices.

TY: Yole is announcing a 3rd consumer technology wave. Can you explain what it is exactly? According to you, how does it impact semiconductor manufacturing processes?

JCE: While the second consumer technology wave was related to smartphones, the third wave is linked to automation and localization. We already have 'robot' vacuum cleaners and lawnmowers, but localization, the IoT, wireless communications including WiFi, 4G and 5G, and navigation systems are delivering more sophisticated applications such as autonomous driving and warehouses. This wave of applications is taking full benefit of new semiconductor content that can provide better imaging, continuous communications, and also pinpoint your location. Thanks to its aging population and early investment, Japan is really ahead in these robotic consumer applications. And of course, in terms of semiconductor manufacturing processes, this third consumer technology wave is driving more semiconductor sales and investment.

TY: Could you please explain how the lithography and bonding equipment at EV Group has evolved to address the ever-increasing MtM device complexity? Could you share with our readers EV Group's vision for the equipment roadmap dedicated to the future MtM devices?

TU: MtM takes place closer to the front end of the line, so processes need to be seamlessly coupled and implemented with FEOL standards. We are just starting to see what is possible by segmenting and adding features to traditional 2D SoCs, largely because MtM is a holistic change in the way we build chips. Therefore, all the areas involved, from design, test, integration, etc., need to be equally harmonized.

At the center of our process solutions roadmap is our emphasis on increasing product performance, mainly driven by the constant increase in interconnect density. In addition, maintaining flexibility in our product platforms is key in order to support our customers' wide-ranging and ever-evolving requirements.

More specifically, in bonding we see thinner wafers and layers needing to be stacked, resulting in increased power requirements for temporary bonding, transfer, and debonding. Where 50µm was a milestone a few years ago, today we are achieving transfer thicknesses well below 10µm, which are used in research and development for applications like advanced logic devices

Another very topical issue for some years now has been hybrid bonding. What started as a wafer-level integration process in image sensors is now becoming mainstream in 3D NAND flash devices, and many other applications see fusion and hybrid bonding as a solution for further performance improvement. In addition, hybrid bonding is seen as the only viable solution for scaling interconnect distances in die-to-wafer bonding below 10µm, where solder systems no longer work reliably. Again, the roadmap shows a rapid reduction in pitch to 2µm, followed closely by the wafer-level interconnect pitch. EVG is the clear market and technology leader in wafer-to-wafer (W2W) hybrid bonding. We have also recently moved into die-to-wafer (D2W) bonding with our strategic partner, ASMPT.

In the area of lithography, we have taken a somewhat disruptive approach. While traditional lithography is mask-based, well suited for the wafer level, we have opted for an all-digital, mask-less exposure technology called MLE to enable chip reconstitution, segmented functionality, etc. The first tool – EVG LITHOSCALE – has been successfully introduced to the market and offers a wide range of functions for wafer-level integration, especially for high-density dies.

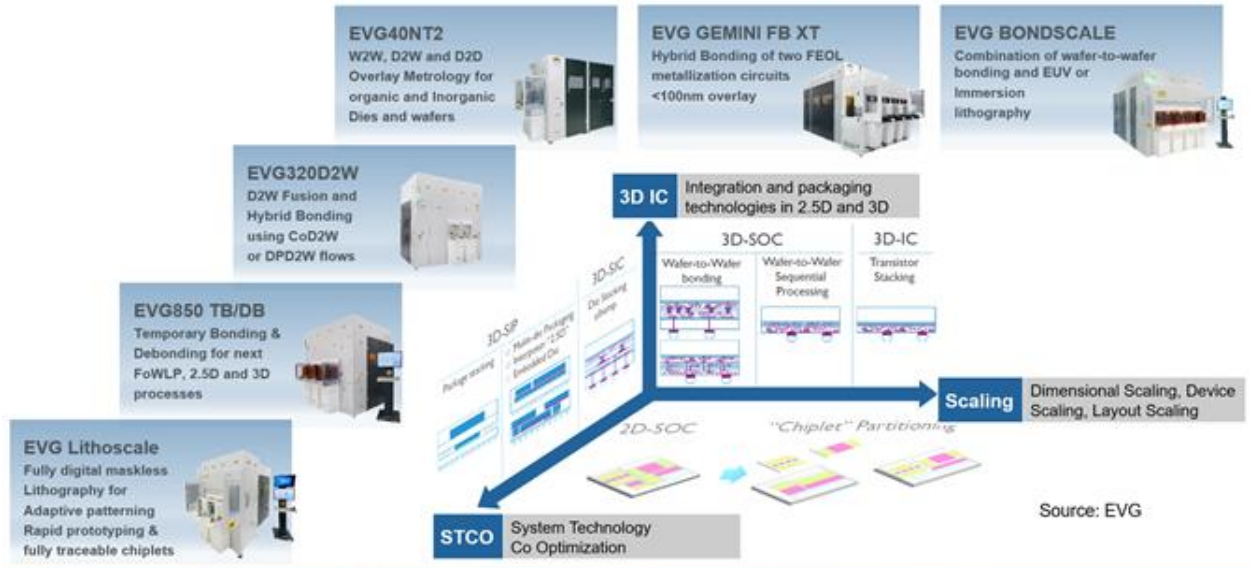
At Yole, we have seen a substantial evolution of the semiconductor manufacturing processes and related equipment. And EV Group has been part of those changes with key technical developments as well as a new business model.

TY: More generally, can you describe the status of the equipment industry facing this progression?

JCE: There's been huge growth in the semiconductor manufacturing equipment market, and this will continue – we expect around 20% market growth next year. However, looking beyond conventional CMOS processing, chip manufacturers are keen to integrate functions at the wafer level, driving growth for companies such as EV Group, which can perform wafer-to-wafer bonding, and die-to-wafer bonding. Bonding technology has already been widely used in CMOS image sensors and is increasingly applied in many memory applications. For example, China's YMTC is using wafer-to-wafer bonding technology in its 3D NAND Flash memory chips. The semiconductor industry cannot scale forever, and there are now many devices that need more than just standard CMOS processing.

TY: EV Group has an impressive product portfolio both in lithography and bonding equipment for the MtM space. Could you explain to the readers the common points in the equipment for bonding and lithography, as well as how these processes are interconnected in the current manufacturing process flow?

TU: Our portfolio is built around several MtM trends and is based on the stage where any kind of heterogeneous integration is taking place.



EV Group's heterogeneous integration solutions portfolio – Courtesy of EV Group, 2022

Looking at the patterning equipment portfolio at EV Group, one cannot miss the recent advancements in maskless lithography and the introduction of the MLE™ exposure system: see Here for more information.

TY: According to you, what is the industry driver for introducing this new patterning equipment? Could you explain the differences between the MLE™ exposure system and the Laser direct imaging systems available in the market?

TU: EVG's MLE technology uses a parallel digital exposure rather than a sequential exposure based on laser dots as in LDI. The key is that MLE chooses an exposure that is very close to what we know today from mask-based systems, including the doses applied to resists and patternable dielectrics. While LDI often faces material issues, MLE is fully compatible with existing infrastructure. In addition, we have developed a fully scalable technology, which is reflected in the first product on the market, EVG LITHOSCALE, where throughput, exposure size, etc., can be scaled according to customer requirements. This means we can match the number of MLE heads to the application, but also scale from small wafers in compound semiconductors to 200mm wafers, such as in MEMS, to 300mm wafers and oversized wafers in advanced packaging without being limited to specific panel sizes – all with the same exposure technology. Therefore, we are not limiting the application of the technology, but die integration and

molded wafers are clearly target applications. The first systems have already been successfully deployed in production.

EV Group is the leader in the bonding equipment market, having more than 70% of the permanent bonding market for MtM devices and dedicated substrates, according to the Bonding and Lithography Equipment for More-than-Moore devices report.

Moreover, many advancements have been unveiled for the wafer-level permanent bonding processes – with hybrid bonding technology for CIS or memory 3D stacking and die-to-wafer bonding technology for 3D heterogeneous integration. At Yole, analysts keep in mind that the equipment for the wafer-level hybrid bonding is already in production and the equipment for die-to-wafer bonding is relatively new.

TY: Could you please provide our readers with an overview of the industry's adoption of permanent bonding technologies and how the equipment can leverage their technical challenges?

TU: W2W hybrid bonding, which involves stacking and electrically connecting wafers from different production lines, is a central process in heterogeneous integration and has a proven track record of success for CMOS image sensors and various memory and logic technologies. However, in cases where the components or dies are not the same size, including the adoption of chiplets in complex chip designs, a D2W hybrid bonding approach may be a more practical option. Several different D2W bonding approaches are being considered for heterogeneous integration, each with distinct advantages and disadvantages (as shown in the table below). Determining which approach is best suited to a given application depends on several factors such as die size, die thickness, total stack height, as well as interface considerations such as contact design and density.

One hybrid D2W bonding method that has already been implemented in volume production for the past few years for applications such as silicon photonics is collective die-to-wafer (Co-D2W) bonding. In Co-D2W bonding, singulated dies are transferred via a carrier wafer to the final wafer and bonded collectively in a single process step. The manufacturing flow for Co-D2W bonding consists of four major processes: carrier preparation, carrier population, wafer bonding (temporary and permanent), and carrier separation.

Another hybrid D2W bonding approach that is beginning to be implemented for heterogeneous integration applications is direct placement die-to-wafer (DP-D2W) bonding, whereby the dies are transferred to the final wafer one at a time using a pick-and-place flip-chip bonder, which consists of three major processes: carrier population, die clean and activation, and direct placement flip-chip.

	Co-D2W	DP-D2W
Transfer Method	Collective Die Transfer by Reconstituted Carrier	Direct Placement of Activated Dies using Flip Chip Bonder
Pros	• Proven technology • Die activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Rework on carrier feasible	• Versatile method • Die thickness invariant
Cons	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	• Bonding interface needs to be touched • Die handling, especially for multi-die stacks such as SRAM, DRAM • Particle management during die placement

Hybrid die-to-wafer bonding approaches for heterogeneous integration – Courtesy EV Group, 2022

EV Group has recently completed a new training facility with a state-of-the-art cleanroom where customers can get training on equipment in a production-like environment. This is also a collaboration area with third-party equipment makers. See the related press announcement here.
TY: Could you describe in more detail the concept of EV Group's Competence Centers (cleanroom training, pilot line?) Do you see the creation of such facilities as a new trend among equipment providers?
TU: We have always been very solution-oriented and strive to work closely with our customers to develop new integration and device applications jointly and be successful. I think the term "innovation incubator" best describes our competence centers. In addition to novel equipment and process demonstrations, MtM has driven demand for the development of complete integration processes such as W2W and D2W hybrid bonding, which typically involve adjacent process steps. Our centers of excellence are very flexible and adapt to customer needs, which can be different for IDMs, OSATs, foundries, and even fabless. Certainly, other companies operate such centers, but the setup at EVG is unique in several ways. The main goal is to provide flexibility and speed of process integration while ensuring the highest level of IP protection at every stage of development. The cleanroom is designed to meet even the most stringent customer requirements and even allows virtual line concepts where wafers are reintroduced into customer fabs for further processing.
TY: How do you see the semiconductor industry evolve? What will be the next steps?
JCE: There are two paths here. We have the conventional CMOS route, which will see TSMC, Samsung, and Intel pushing the limits of the 5 nm, 3 nm, 2 nm nodes, and so on – they will keep this up for the next 15 to 20 years. We also have the MtM path, which is creating an incredible amount of business. Here we have LEDs, power management, and RF devices being manufactured from materials such as GaAs, SiC, GaN, and silicon-on-insulator that can provide better performance than silicon. These 'new' materials were once only found in niche markets but are now being used to manufacture semiconductors at high volumes with yields and reliability to match CMOS production. Silicon will remain the key material for the semiconductor industry, but these alternative materials will capture between 15 and 25% of the market in the next five years. And this strong push to make these once niche materials mainstream will generate a lot of business for everybody.

Interviewees

Dr. Thomas Uhrmann is director of business development at EV Group (EVG) where he is responsible for overseeing all aspects of EVG's worldwide business development. Specifically, he is focused on 3D integration, MEMS, LEDs and a number of emerging markets. Prior to this role, Uhrmann was business development manager for 3D and Advanced Packaging as well as Compound Semiconductors and Si-based Power Devices at EV Group. He holds an engineering degree in mechatronics from the University of Applied Sciences in Regensburg and a PhD in semiconductor physics from Vienna University of Technology.

Jean-Christophe Eloy is President and CEO of the Yole Développement company. Created in 1998, the market research & strategy consulting company has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. His mission is to oversee the strategic direction of Yole Group of Companies.

With System Plus Consulting, Blumorpho, PISEO and Yole Développement, Yole Group of Companies has developed a unique understanding of technologies to accurately evaluate markets, applications, solutions and strategies.

With more than 70 analysts, including PhD and MBA qualified industry veterans, the group collects information, identifies trends, challenges, emerging markets, and competitive environments and then turns that information into results to give a complete picture of the industry's landscape.

All year long, Jean-Christophe builds deep relationships with leading semiconductor companies, discussing and sharing information across his global network. His aim is to get a comprehensive understanding of their strengths and guide their success.

Interviewer

Taguhi Yeghoyan PhD., is a Technology & Market Analyst, Semiconductor Manufacturing at Yole Développement (Yole), within the Semiconductor, Memory & Computing division.

Taguhi's mission is to follow daily the semiconductor industry and its evolution. Based on her expertise in this field, especially on the semiconductor value chain (processes, materials, equipment, and related applications), Taguhi performs technology & market reports and is engaged in dedicated custom projects.

Prior to Yole, she worked in world-class European research centers and laboratories, including imec (Belgium), LMI (Lyon, France) and LTM at CEA Leti (Grenoble, France). All along her past experiences, Taguhi has authored or co-authored one patent and more than nine papers.

She has graduated from Wroclaw University of Technology (Poland) and University of Lyon (France). Taguhi also completed her PhD. in Material Science from the University of Lyon (France).

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