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Building Better Bridges In Advanced Packaging – September 21, 2023

Building Better Bridges In Advanced Packaging

Leading-edge applications, from biotech to co-packaged optics, require choices in architectures,

assembly methods, and materials for system performance.
SEPTEMBER 21ST, 2023 - BY: **LAURA PETERS**

The increasing challenges and rising cost of logic scaling, along with demands for an increasing number of features, are pushing more companies into advanced packaging. And while that opens up a slew of new options, it also is causing widespread confusion over what works best for different processes and technologies.

At its core, advanced packaging depends on reliable interconnects, well-defined signal paths, and minimization of nuisance effects like insertion losses, interconnect crosstalk, substrate warpage, and hot spots in the system. Those parameters can vary significantly depending on the choice of package, which can be anything from 2.5D, fan-out chip-on-substrate (FOCoS), 3D-ICs, or bridges that may be used separately or in conjunction with the other approaches.

And that's just for starters. Semiconductor packaging roadmaps emphasize robust interfaces at every turn, but which one is right for a particular application isn't always clear because there are many ways to get to a final result. There are a slew of new processes too, including wafer-to-wafer bonding, backside power distribution, and co-packaging optics in packages. Silicon interposers (bridges) provide the highest bandwidth communications, while organic interposers are drastically less expensive and can embed passives along the interconnect route from RDL to C4 bumping.

New materials and architectures

Since the invention of the first IC, engineers have debated the fundamentals of one material versus another. In the early days it was silicon versus germanium semiconductors, always with the end goal of making cost-effective electronics. Silicon's abundance and its ability to grow a native oxide eased integration and ensured reliability, making it the substrate of choice.

Fast forward to today and manufacturability in advanced packaging is undergoing a similar metamorphosis that ASICs once did. In medical, biotech, HPC, mobile, and 5G/6G, engineers are returning to physical and chemical principles to determine the best way to combine photonics, microelectronics, silicon bridges with redistribution layers, and chip communications with medical electronics.

The trick is designing chips to packages using a robust architecture that withstands temperature stress cycles and endures a specific use case.

At the same time, chipmakers are under pressure to deliver system-level modules sooner. Ironically, this calls for lower-temperature processes in some cases to effectively embed devices closer together and into new places, such as the human body.

“There are only so many metals that we can use for implantable devices, like gold, platinum, and some chromium steels. We can use aluminum oxide, but few polymers are suitable when exposed to organic media,” said Dick Otte, CEO of Promex. Existing processes can be engineered for such new applications as implantable medical devices or single-use testers to detect glucose levels or a pathogen such as a Covid virus.

In high-performance computing, problems arising from warpage and stress fluctuations caused by temperature cycling are driving a wholesale change from organic substrates to glass. Intel recently announced prototypes of chips on glass substrate that provide a path to continued feature scaling and improved power delivery in high-performance systems (see figure 1).

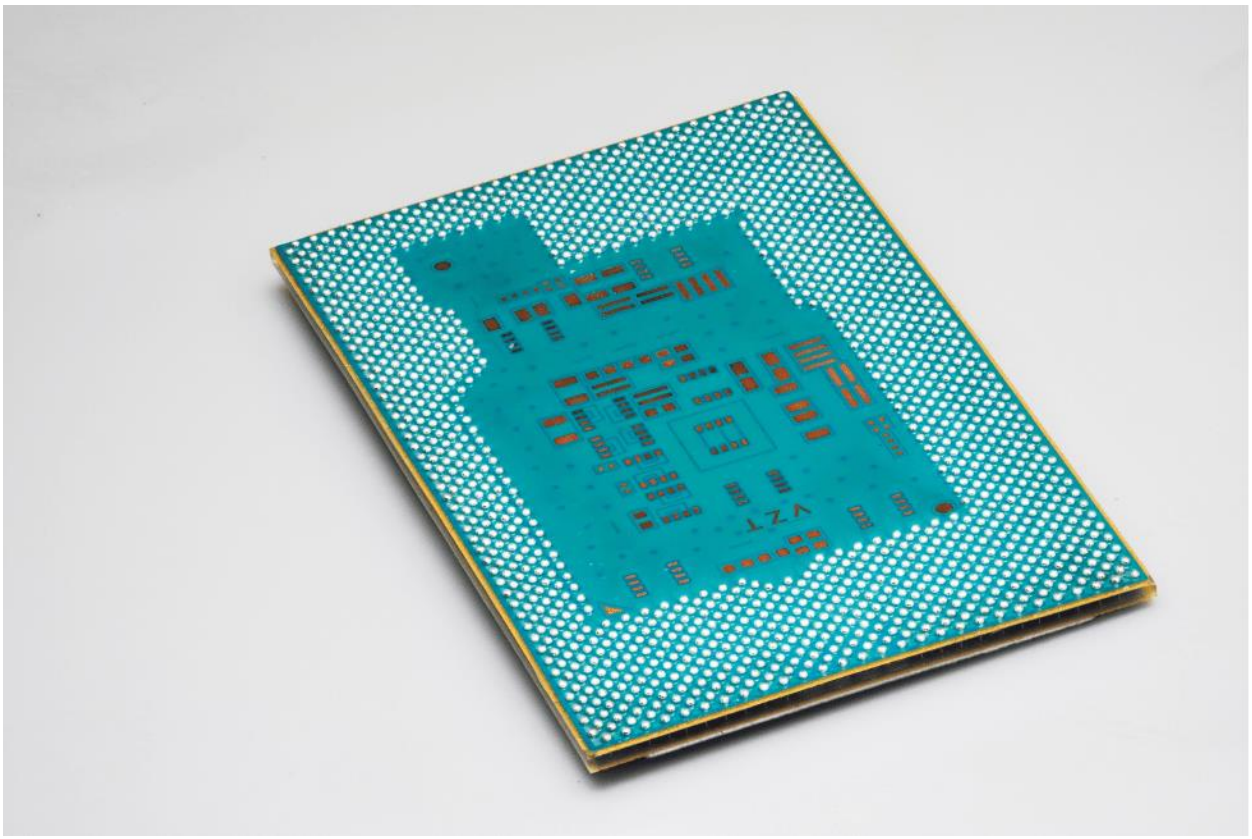

Fig. 1: BGA side of an assembled glass substrate test chip. Source: Intel

In lieu of rigid glass substrates, fan-out approaches with silicon bridges are reducing the need for costly multi-layer laminate substrates, which have been in short supply in recent years. A silicon bridge can be thought of as the best combination of the side-by-side 2D approaches with fan-out chip on substrate, FOCoS (see figure 2).

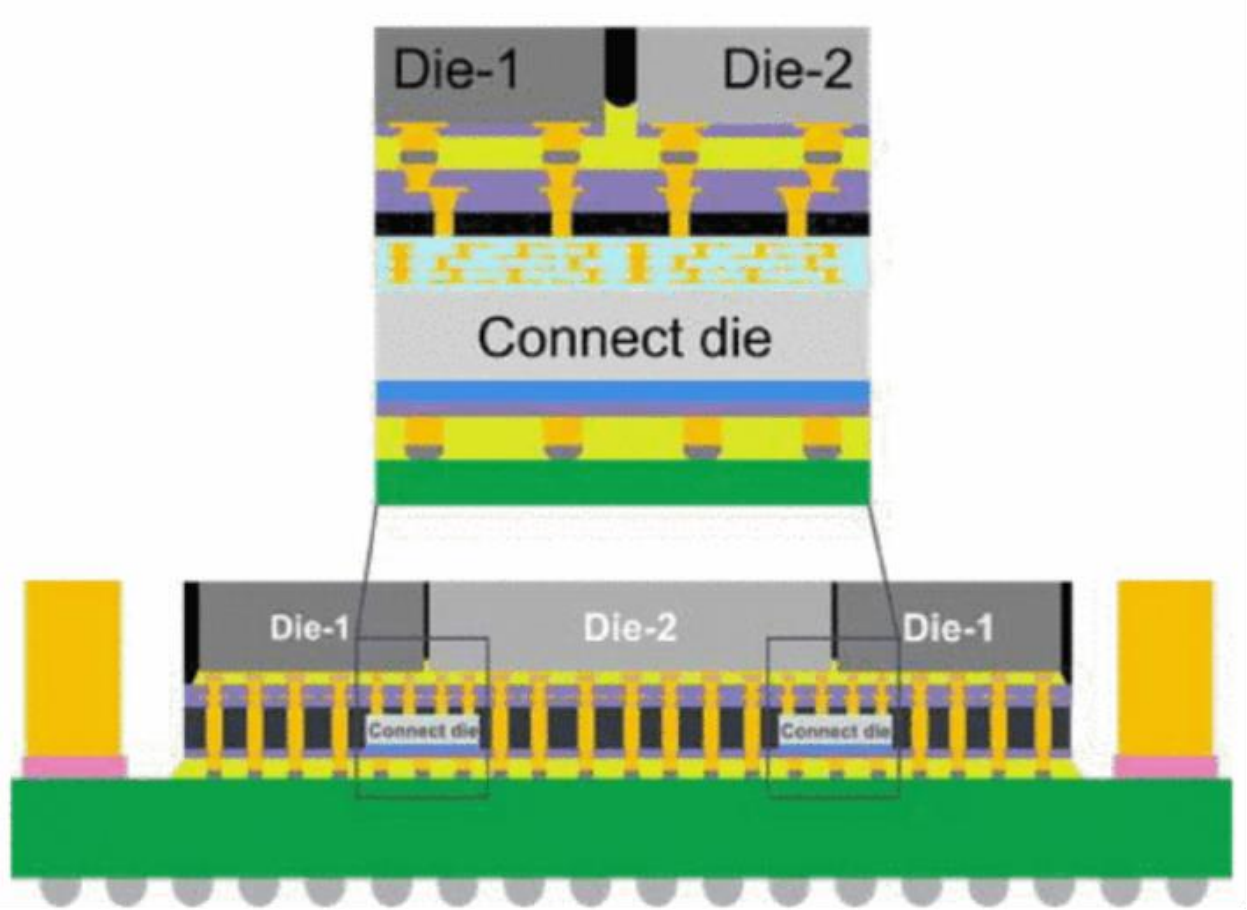

Fig. 2: When integrating high-bandwidth silicon bridge (0.5µm lines and spaces), warpage of the system depends on die thickness (450 to 650µm), mold area, and CTE of the epoxy molding compound. Source: Amkor

Bridge methods deliver other benefits on the performance side. “In bridge-die connections, the signal path benefits from having little distance between dies, on the order of 1 to 2 millimeters, so they can communicate well electrically,” said Mike Kelly, vice president of Advanced Packaging and Integration at Amkor. “It’s a more complicated system mechanically and from a reliability standpoint, and we can have mixed functionality like RF and logic in a package.”

It’s becoming clear that silicon interposer bridges must be as small as possible because of costs. An analysis by Amkor engineers revealed that thinner active dies in the FOCoS bridge construct are more susceptible to warpage. The work also pointed to the positive effects of using molding compounds with a lower coefficient of thermal expansion (CTE) molding compound as a second-order effect. [1]

Redistribution layers with wider lines and spaces (to 2µm L/S) manage the second tier of interconnect speed inside these packages. Overall, the thermal dissipation path out of the top of such large systems (beyond 3X reticle size) will call for even higher conductivity to remove heat than existing thermal interface materials (TIMs). Eventually, metal TIMs will likely be needed.

Put simply, closely spaced logic chips tend to heat up like one large logic chip in a package, with HBM positioned on the system perimeter. This is why ASE is promoting its bridge technology, noting that the silicon interposer (copper/SiO_2) layers on the order of 1µm lines and spaces tending to cause higher insertion losses and crosstalk between copper lines than in FOCoS interposers, which have wider copper

and polyimide dimensions (3 to 4µm). A key advantage, in addition to the high-bandwidth, high-speed communication in silicon interposers, is the flexibility in die routing for ground traces around the I/O signals, which reduces the crosstalk. [2]

As a result, engineers and package designers have options within the 2.5D, FOCoS, and FOCoS-bridge technologies to weigh layout density, electrical/thermal/stress performance, and cost depending on the module's specific application (see figure 3), as summarized by ASE engineers. "It can be expected that the size of advanced packaging will become larger and larger, and the warpage and stress performance during the assembly process will become more important," they said.

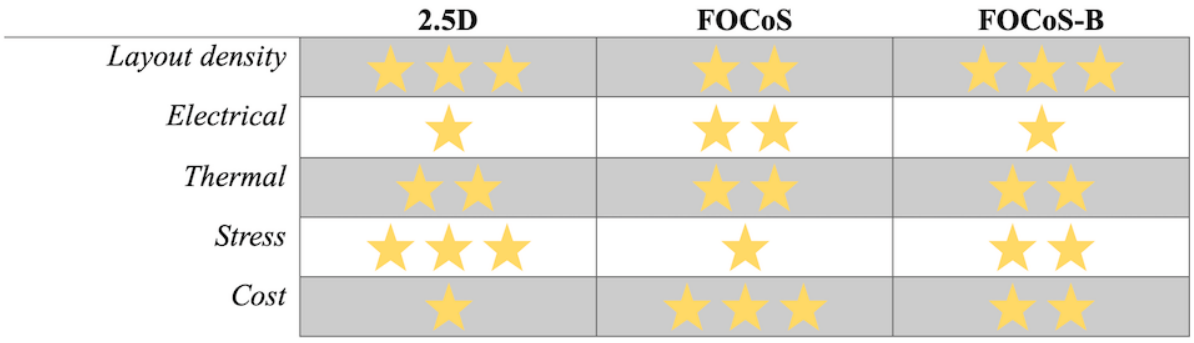

Fig. 3: The different attributes of 2.5D, FOCoS, and bridge technologies. A bridge manages stresses better than FOCoS, but not as well as 2.5D approaches. Source: ASE

Simultaneously, co-packaged optics is coming soon to data centers. Intel's Babak Sabi, senior vice president of assembly test technology development at Intel, held up a connector with optical inputs at a panel discussion at the recent Semicon West. "Packaging is all about interconnects, and we're bringing together lots of cores and memory, and people are talking about wafer-level integration of products," he said. "This is where the glass substrate is extremely important, because we can completely eliminate the interposer."

In addition to a roadmap to incorporating glass substrates for better performance and large-scale warpage control, Sabi talked about optical interconnect adoption. "By the end of this decade, we're going to start seeing optical in many different formats," he said, noting that Intel and its partners are working on a "standard" connector for optical interfaces to chips. He used the analogy of a connection consumers are very familiar with — USB-C. For hyperscale networks, an industry standard optical connector can eliminate the dangling fibers and semi-automated approaches of connecting to silicon photonics today, enabling superior manufacturability and automation.

The need to integrate front-end wafer processing with advanced packaging is driving process development changes too. Applied Materials recently presented its roadmap to co-develop hybrid bonding and advanced die placement tools from different suppliers with Applied's latest vacuum-based multi-chamber platform. The need to integrate processes like CMP with hybrid bonding and advanced placement tools, for instance, is giving rise to partnerships between Applied, EV Group, and BESI, and it's happening among other suppliers and R&D hubs globally.

How thin can wafers and devices go?

All of these developments require thinner silicon wafers, which in turn allow for slimmer cellphones, watches, and implantable devices, among other things.

That also makes them harder to work with, and more prone to process variation and defects. But wafers must be thinned out for 3D device-level integration, and they will require new types of interconnects, such as hybrid bonding, a technology pioneered by Sony with CMOS image sensors. In general, wafers are being thinned from around 600 to 50 µm and below.

Progress from millimeter-sized devices to smaller microLEDs or microOLEDs that fit on the rims of glasses, and disposable biotech testers, requires new ways of looking at assembly, as well. And while it looks like silicon interposers will remain safely in the domain of fabs, the OSATs, material, and equipment suppliers are collaborating to deliver new or substantially modified processes.

“In biotech, there’s a lot of complex chemistry involved because they’re utilizing some kind of molecular interaction — which the electronics, chemistry, or MEMS detect and try to match — showing that a pathogen is present or not,” said Promex’s Otte. “So, we modified the assembly process to avoid damaging those parts, by developing a room-temperature curing process, for example.”

Otte explained that because biotech devices interact with the patient, and then send signals to the outside world, they cannot undergo standard semiconductor processes, such as 220°C mass reflow, exposure to UV light, or ultrasonic agitation in deionized water. Development to specifications in biotech or medical electronics can take two or more years to meet specifications, and modules typically require mechanical structures (microfluidics) that cannot be exposed to water. Such new requirements will continue to drive new processes

Backside power, hybrid bonding, and new materials
Other changes are afoot, as well. Fundamentally, what gets used comes down to physics, chemistry, device performance, and cost, but that includes a lot of options that can be tailored for a specific application or use case.

Backside power delivery will appear first in the highest-performing chips. This approach places power delivery to transistors on the wafer backside, which require wider interconnects, while only signal lines are carried on the frontside of the devices, optimizing CD for the application. BPD can improve reliability while paving the way to integrating simple devices on the backside as well.

BPD and hybrid bonding are two of the hottest topics today in semiconductors. Each includes various approaches, and those approaches involve different levels of complexity. The same goes for carriers made out of silicon wafers or glass, each of which has pros and cons. Glass, for example, is very flat and is typically re-used in carrier applications.

Another relatively new process is carrier debonding to enable thin wafer processing. In a recent work, imec and Brewer Science revealed the details of a glass carrier de-bonding process being optimized for ultrathin wafers (50µm to 20µm). [3] On 300mm glass wafers, engineers combined three chemistries including an edge-bead remover, temporary bonding material, and a release layer that were optimized for clean release of thin 300mm silicon wafers from a carrier using a mechanical (blade) release mechanism.

The process was optimized to ensure compatibility with wafer backside oxides and dual damascene processing, while preventing unintended wafer adhesion loss or contamination, while meeting across-wafer thickness variation (TTV) specifications. Enabling thin wafer release is just one of many processes, that are important to making backside power distribution approaches work.

Conclusion
As OSATs gain experience with integrating new bridge technologies, the approach can deliver performance and cost benefits that are between FOCoS and 2.5D integration approaches — expanding the options available to designers. Use of these high density packaging approaches is still restricted, however, to chipmakers with in-house wafer-to-package levels of integration.

Meanwhile, engineers are devising creative solutions to assembling biotech and medical electronics.

Companies are collaborating to better bridge wafer fab and assembly and packaging worlds. Bonding and debonding of wafer and glass carriers will likely play an increasing role as chipmakers continue to combine layers in three dimensional devices.

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