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Improving Redistribution Layers for Fan-out Packages And SiPs – September 15, 2022

Improving Redistribution Layers For Fan-Out Packages And SiPs

Good adhesion, stress management, and warpage control are features of high performing RDLs.
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Redistribution layers (RDLs) are used throughout advanced packaging schemes today including fan-out packages, fan-out chip on substrate approaches, fan-out package-on-package, silicon photonics, and 2.5D/3D integrated approaches. The industry is embracing a variety of fan-out packages especially because they deliver design flexibility, very small footprint, and cost-effective electrical connectivity to a multitude of I/Os using RDLs.

“Right now there is strong interest in heterogenous integration of chiplets leveraging advanced RDL structures involving 2.5D fan-out on substrates with copper pillars, as in ASE’s FOCoS approach. I/O requirements for this type of approach range from a few thousand to over a hundred thousand I/Os,” said Mark Gerber, senior director, engineering and technical marketing at ASE.

In particular, high-performance computing, data servers, AI, and 5G applications encouraged development of packaging platforms combining substrates with fan-out on as well as embedded bridge technologies, with most of the processes integrated at OSATs. For instance, a recent TechSearch International analysis of AMD’s elevated fanout bridge (EFB) GPU package, a fan-out on substrate approach, highlighted the OSAT’s strong play in high performance packaging.

With advanced packaging being performed at OSATs, IDMs, and foundries, competition is heating up for high-end packaging. For multichiplet integrated packages, RDLs scale from the 10µm line and space range to a state-of-the-art of 2µm lines and spaces (L/S) level. To manage complex interactions, advanced modeling, materials engineering, and wafer processes are coming into use to ensure robust RDL fabrication.

Issues in advanced fan-out and heterogenous packages include die shift, die warpage, die-to-die stress, and the risk of broken RDL traces. RDL processes involve the plating of copper inside narrow traces in organic polyimide (PI) or polybenzoxazole (PBO) films. New processes are designed to improve RDL adhesion while reduce mechanical and thermal stresses during thermal cycling.

OSATs including ASE, Amkor, and JCET offer many package types with advanced RDL processes.

According to Mike Kelly, vice president, advanced package and technology integration at Amkor, 4-layer RDL are mature at with yields have reached the 99% level. “Four-layer RDL is needed for an HBM data bus, and we estimate about 85% of packaging needs can be met with 4-layer RDL over the next several years.”

Directions in advanced packaging

A variety of advanced packages have been coming to the fore since the slowing of Moore’s law at around

14nm met with a need for greater functionality on SOCs. Heterogenous integrated packages have gotten increasingly popular since then, meeting application needs in deep learning, networking, and CPUs/GPUs for personal computing applications. For instance, ASE's VIPack platform has six RDL-based product families that address application-specific requirements, including the fan-out chip on substrate (FOCoS), the FOPoP and the FOSiP.

Indeed, at the most recent IEEE ECTC, many chipmakers revealed new fan-out packaging designs. In particular, chip-last integration schemes that reserve known good die placement for later in the process, are gaining momentum, processes that begin with RDL formation on a carrier.

Rise of chip last

Temporary bonding and release layers, such as the Brewer Science BrewerBOND materials, enable RDL processing on carriers followed by a laser release step. RDL first, also known as chip last fan-out flow, enable high yield and lower overall cost while ensuring placement of known good die on known good RDL.

Samsung's Taewon Yoo and colleagues presented a chip-last FOWLP scheme at ECTC and compared results directly to the equivalent a substrate flip-chip BGA and interposer package-on-package approaches.[1] The FOWLP process uses a memory on logic device configuration, achieving good electrical and thermal performance with a "thickness is generally half the size of substrates when RDL is formed directly on top of I/O pads." Samsung noted the design enables a shorter electrical signal path than in the FCBGA and a final package thickness was 0.26mm.

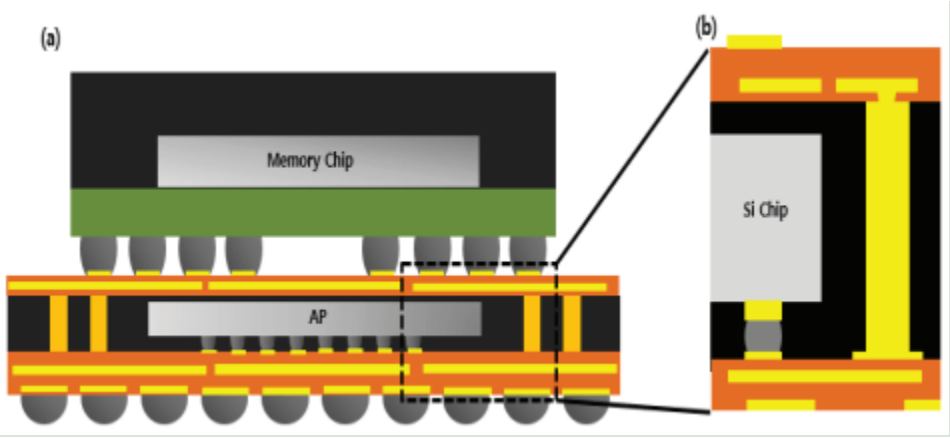

Fig. 1: The chip last, fan out WLP reduces package thickness by 50% relative to FCBGA and PoP architectures. Source: Samsung [1]

In Samsung's design (see figure 1), the RDL is built on a glass wafer carrier. This approach also utilizes through-mold copper posts that connect the frontside and backside RDLs. The RDLs feature 8µm plated copper lines in 7µm polyimide spaces. "Thickness of this RDL is generally half the size of substrates and is formed on top of the I/O pads," stated Taewon Yoo of Samsung Electronics.[1] The fan-out approach also dissipates heat more efficiently than the PoP approach in this case. The engineers were able to relive stress, which concentrated under the solder balls, by modifying the RDL design under the top passivation.

Placement accuracy and die shift are well known issues in multi-chiplet packaging. RDL first fan-out approaches can help. "For the strategy of die shift improvement, fine pitch requirements, process optimization and known good die (KGD) yield management, RDL first (also called chip last) is a candidate to effective cost reduction," as highlighted in an ECTC presentation. [2] Jen-Hsien Wong and colleagues at ASE optimized the chip-last strategy for 8 chips in a 50 x 35mm FO die surrounded by epoxy molded

compound with FOCoS with different trace layouts. Thermo-mechanical modeling considered CTEs of all materials (silicon die, RDL, heat spreaders) as a function of temperature, in addition to material modulus. A finite element model calculated stress in the die-to-die gap region where CTE mismatch tends to be high. The heat spreader provides heat dissipation but also helps in minimizing package warpage. The final optimization reduced trace stress under the die-to-die gap region by 34% and produced the optimal layout.

The study highlighted that modeling package warpage behavior between room temperature and high temperature (260°C) allows superior heat spreader design. The approach provides guidance for warpage control and future thermal-mechanical optimization of multichip packages using chip last FOCoS.

RDL process flows

A key enabling technology that brought FOWLP to the forefront was the formulation of low temperature, photo-imageable polyimides such as the LTC Series from Fujifilm, according to Thomas Uhrmann, director of business development at EV Group. Other polyimide manufacturers include Asahi and Hitachi Dupont. The latest processes are using vacuum curing of polyimide (PI) or polybenzoxazole (PBO) films to provide superior dielectric film properties while also speeding cure times for high-volume manufacturing.

RDL flows typically involve semi-additive processes that includes dielectric deposition, wet or dry etch, barrier and seed layer deposition, and copper plating. Fan-out WLP, but for high density RDL, dual damascene processes are increasingly attractive to avoid issues of seed layer undercut and sidewall etch vulnerabilities associated with semi-additive process.[3] By embedding the trace in the dielectric layer without an etch step, and employing a dual damascene process, copper collapse risk was eliminated and the new RDL improved the interconnect reliability. In the new process, via and RDL patterns were formed in the organic dielectric using a single lithography exposure step. The new 4-layer RDL (see figure 2) features 2/1µm lines/spaces. Process modification to improve the thickness uniformity of the dielectric was able to reduce shorting caused by thick copper remaining at the wafer edge.

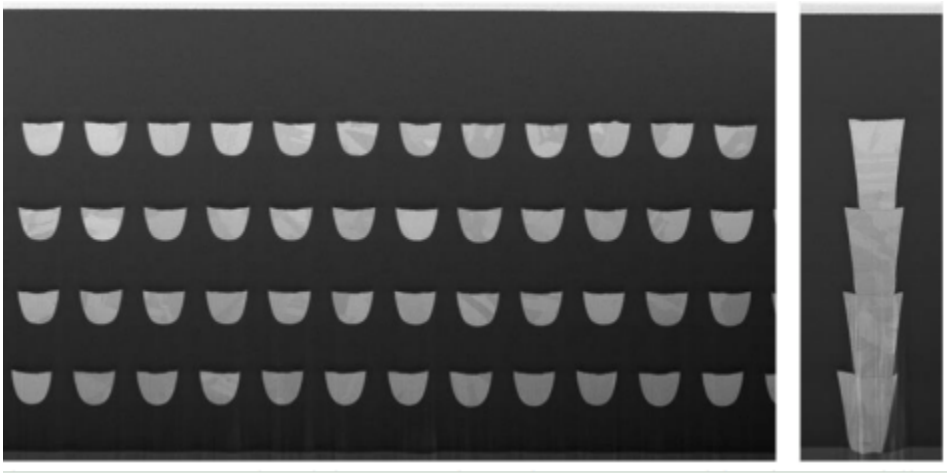

Fig. 2: The 4-layer RDL with 2/1µm L/S and 2µm via stack. Source: Amkor [3]

Conclusions

RDL processes are relatively straightforward, but once they are integrated with complex processes involving multiple chiplets, significant optimization become necessary to manage the CTE mismatch, electrical, thermal, and mechanical behavior in these systems in package.

References

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