SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Challenges With Chiplets And Packaging– September 15, 2021

Experts at the Table: The impact of optics, copper hybrid bonding, more standardized interconnects, and many other technologies under development.

SEPTEMBER 15TH, 2021 - BY: **MARK LAPEDUS**

Semiconductor Engineering sat down to discuss IC packaging technology trends, chiplets, shortages and other topics with William Chen, a fellow at ASE; Michael Kelly, vice president of advanced packaging development and integration at Amkor; Richard Otte, president and CEO of Promex, the parent company of QP Technologies; Michael Liu, senior director of global technical marketing at JCET; and Thomas Uhrmann, director of business development at EV Group. What follows are excerpts of that conversation. To view part one of this discussion, click here.

SE: What are some of the emerging technologies you see out there?

Otte: One is the co-package of optics. We're moving in that direction. It looks like somewhere around the 50-terabit data rate onto and off of a chip is what's going to force optics. You can't get enough area to do it with electronics. You must go to optics, which has a shorter wavelength and holds the evanescent fields in close. With optics, cross talk is eliminated. Incorporating optics is a complicated thing. One of the things it is going to do is exacerbate the time to market issue. We have to find ways to do these new higher-functionality technologies quickly, meaning in less time. You have to do this in days versus weeks and months, which is what it now takes when you have to run things through fabs.

SE: Chiplets is also a hot topic. With this methodology, a vendor may have a menu of modular dies, or chiplets, in a library. Chiplets can have different functions and process nodes. Customers can mix-and-match the chiplets, and then assemble them in an existing advanced package or a new architecture. The goal is to speed up time to market and reduce the cost. How do you see this working out for the industry?

Otte: As we go to chiplets, it's clear that the first applications are going to be high-end systems. It's all going to be custom. There will be a lot of specialized parts here. Now, what happens in 5 to 10 years? Will full custom continue to be the case, and is the high end the only place for chiplets? Or are they going to get commoditized? Will they be sold in catalogs? If that's where we're headed, that means we may need a whole set of new standards for configurations, spacing and interconnect techniques. That's not a six-month event. This is a multi-year activity. My view is that it's going to evolve that way. It's only a matter of time and how fast that happens. And if anything has ever surprised me about this industry in my years of association with it, it's how everything starts to happen faster and faster. As soon as it becomes possible, somebody does it. One of the things that's going to happen in the next couple of years is companies will start selling chiplets. They will introduce catalogs of these devices with standard functionality. And then the question is, where do you get the substrates to integrate the devices? How are we going to enable interconnects for these devices? And are we going to be driving these things down to 10µm pitch bumps, or are we going to stay at 50µm where we are now?

Kelly: Chiplets are a fascinating discussion area these days. A couple of things come to mind in imagining all the marketplaces that eventually can use a chiplet heterogeneous approach. It always starts out with high performance. Chiplets, in this case, are enabling differentiation in product architectures. But we're in the very early phases of this. Just the leading companies are participating in it, and their chiplets are quite specialized. They are an integral part of how the architecture is done for their entire product, and it's fiercely competitive. So every ounce of performance they are getting is a difference in getting new

business or not. That's the first class of chiplets, and that's where we are today. What those companies are doing today is creating a design and manufacturing infrastructure to support the use of heterogeneous integration. All of this will be the foundation for all the other product segments that will eventually go this way, as well. There will be new product classes that enable an architectural differentiation and time to market. It ensures you have the adequate functionality and performance at the lowest possible cost. And if that infrastructure is in place for manufacturing, then having a chiplet catalog will make a lot of sense. This process needs to be time phased. Early on, it will be the high-performance companies. They have some differentiated ways they're approaching their chiplets strategies. They are all good and they're all competitive.

Chen: When we talk about chiplets, it's a case of system optimization from co-design all the way to packaging, assembly and test. On the one hand, the packaging engineer or packaging architect needs to work with foundries and IDMs. On the other hand, they also need to look into the future in terms of products and systems. The packaging engineer or architect needs to communicate across both sides and work together in the co-design process to optimize performance, manufacturing and test. When we talk about co-design, it is not just the electrical design. It is the physical design and layout, including thermal, mechanical, and reliability, and the physical optimization in terms of time-to-market and cost. It's important to look at the next few product cycles. How can we do it this initially? And how can we do the next few product cycles? There's a few examples that we can learn from. We can learn from chiplet products from leading fabless and IDMs. Both of them have a different approach, but both of them are looking at it from an overall perspective. They are not just looking at one product, one device node, at one point in time. And if we look at packaging innovation, we talk about flip-chip, silicon bridge, fan-out, silicon interposer, and 3D stacking. The silicon bridge was introduced by an IDM who designed chiplets from the beginning. The co-design process needs to start at the very beginning. But on the other hand, there are innovations in high-density fan-out and substrates where the requirements are a little different. While we discuss these different working models for chiplets, it is important to consider and engage with the whole ecosystem.

Liu: I'd like to recommend that we all look into the value chain of the whole chiplet business model. JCET Group is part of the Open Domain-Specific Architecture (ODSA) sub-project within the Open Compute Project (OCP). At OCP ODSA, we are focused on investigating the readiness for chiplets. When thinking up a practicable business model for commercializing chiplets, the team drew a few interesting analogies to successful businesses, including but not limited to IKEA. That's indeed an ongoing development, and we will likely end up with more than one chiplet business model. I strongly recommend everyone to drop by and get involved in activities hosted by OCP ODSA.

Chen: I'm leading the Heterogeneous Integration Roadmap. We have 23 different chapters. The important thing about having 23 different chapters is that it really does take a whole village. Everyone in the village needs to contribute. Otherwise, one may miss something important, and subsequently miss the product launch. It truly takes the whole heterogenous integration village, whether you want to innovate automotive, high-performance computing, 5G, IoT, or medical and health wearable products. While we speak about packaging and assembly, we must also think about wirebond. Wirebond is a very important part of our industry. Wirebond unit volumes continue to grow. It's not growing as fast as flip-chip, but the number of units continues to grow. There is a tremendous number of smart wirebond engineers, and they are still innovating. We are a very innovative industry. Now we need to innovate on physical design for chiplets in heterogenous integration.

SE: What are your big concerns about chiplets?

Chen: For chiplets to become pervasive in the future, an open business model will be crucial. And for both the business model and market to be effective, the full technology ecosystem needs to be there to serve them.

Otte: There are several issues and questions here. For example, will we be able to use chiplets for small-volume jobs, or will the one-time design and tooling costs limit them to high-volume applications? What will the cost of product built with chiplets be? What will the chiplet supply chain look like? What chiplet mounting and interconnect method will dominate in the long run among the various versions being introduced? Who will design and fabricate silicon-based interposers if they dominate as it likely seems? Who will set the chiplet electrical and mechanical standards? What new assembly and test processes and related equipment will be needed? Will current design software adopt to chiplets or will new packages be needed?

Liu: Let me rank my top concerns about chiplets: (1) unclear value chains and business models; (2) reliability, test and repair warrant issues; (3) multiple standards and resource optimization; (4) chiplet power delivery and thermal challenges; and (5) chiplet signal integrity plus EMI-shielding issues.

SE: For chiplets and other advanced packages, customers must decide whether to design their next high-end packages using existing microbump interconnects or move to a higher-density technology called copper hybrid bonding. Some may implement both approaches. How far can we scale the pitches for traditional microbumps? And what are some of the challenges as we move beyond today's 40µm bump pitches?

Uhrmann: The industry consensus is that below 20µm bump pitches, the connection of dies is becoming rather difficult using reflowable solder-based connections. Mainly, the liquid nature during soldering is introducing major challenges and prohibits the process from scaling further. Around 10µm pitch is the insertion point of hybrid bonding. For this, the connection is done purely based on the instantaneous bonding between oxide layers, and the electrical connection is done via annealing and the copper expansion and diffusion at elevated temperatures. The interface stays solid during the whole process. This means there is virtually no limit in scaling from a material point of view. For wafer-to-wafer bonding, 500nm pitch has been demonstrated by EVG and Imec, where the challenge is now to transfer the process onto the die level. Microbumps present challenges for material suppliers of chemistry for plating, pre-applied underfill, and resist materials in order to optimize the structure of the bumps. This now becomes an engineering challenge for the capital equipment industry.

SE: The industry is also talking about going to copper hybrid bonding to enable chiplet-like architectures at fine pitches. What are the issues here?

Kelly: Regarding 3D and copper-to-copper bonding, it's coming. We've already seen product announcements using this kind of bonding. It will likely be things like SRAM first, where a lot of L3 cache is needed in a product. The easiest way to incorporate this is by putting another die on top, rather than blowing the die size up and affecting yields and cost structure. Once again, high-performance is driving chiplets in the early stages. Eventually, we'll get to a place where it will make sense for a lot of other product markets. We could even see chiplets and wirebond, if that's the lowest possible way to integrate several die and meet electrical performance requirements.

Uhrmann: Hybrid bonding has been an industry standard process at wafer level already for more than five years. Here, hybrid bonding is seen as an integral part of the device manufacturing process. The big difference with today's requirements is the drive to introduce hybrid bonding in high-pitch interconnects into heterogeneous integration and consequently into a more packaging-like environment. One of the main drivers for chiplets is the heterogeneous nature of joining dies from different sizes, manufacturing sources, technology nodes, and functions, which means the wafers need to be diced at first. As hybrid bonding is based on ultra-clean, ultra-smooth, literally nanometer-perfect surfaces, these surfaces need to be conserved during dicing, driving the adoption of plasma dicing for chiplets. The same is true for the chip-edge quality without any microcracks and straight sidewalls, where plasma dicing becomes a must. After separation of the dies, the placement becomes the next crucial process, where cleanliness, speed, as well as accuracy need to be united in a process step. For die-to-wafer (D2W) bonding, two possible integration flows are developed — bonding dies individually one by one, or as a collective using a die

carrier. The first direct-placement D2W (DP-D2W) approach uses dies mounted on dicing tape or on a specific die carrier to run through die cleaning and plasma activation in one tool or part of a die bonding cluster. Then, it hands off the clean dies in the same way as the cleaned and activated wafer in the D2W bonder for population. For collective D2W (Co-D2W) bonding, die population is done on an auxiliary wafer, placing the dies face up on an adhesive layer. In this case, the dies can still be protected during placement, allowing faster placement of the dies with more relaxed requirements to the die bonder. Subsequently, the die carrier is processed the same way as in a W2W bond cluster that is industry standard today.

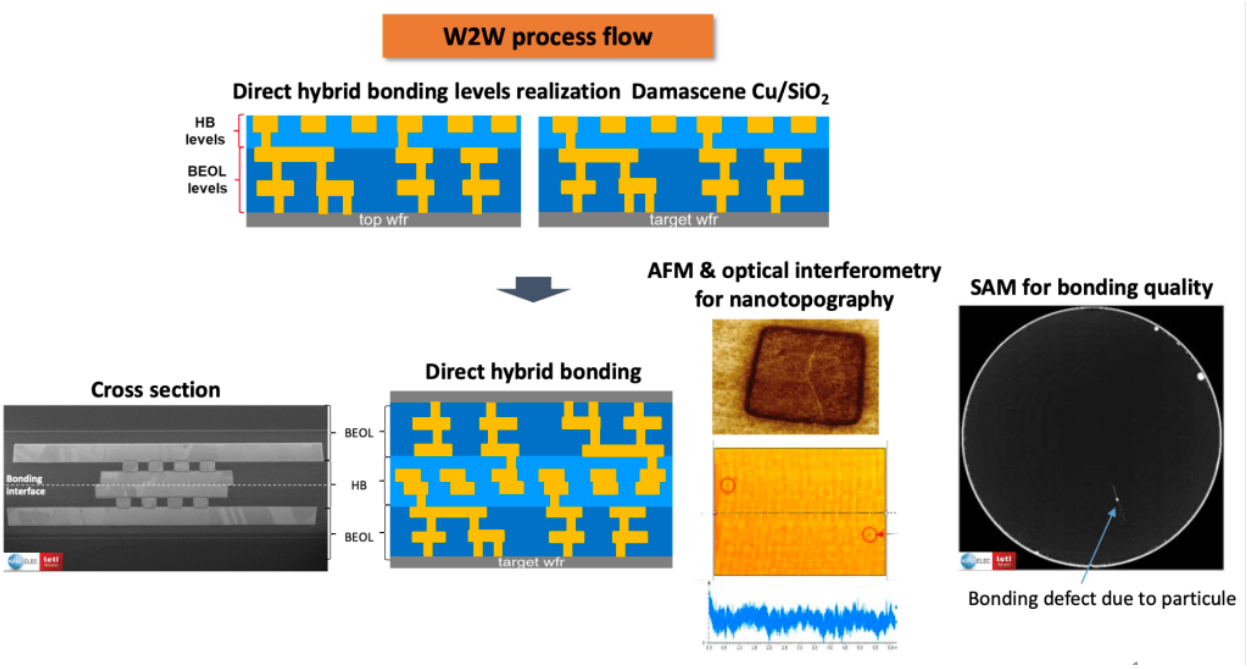

Fig. 1: Hybrid bonding flow. Source: Leti

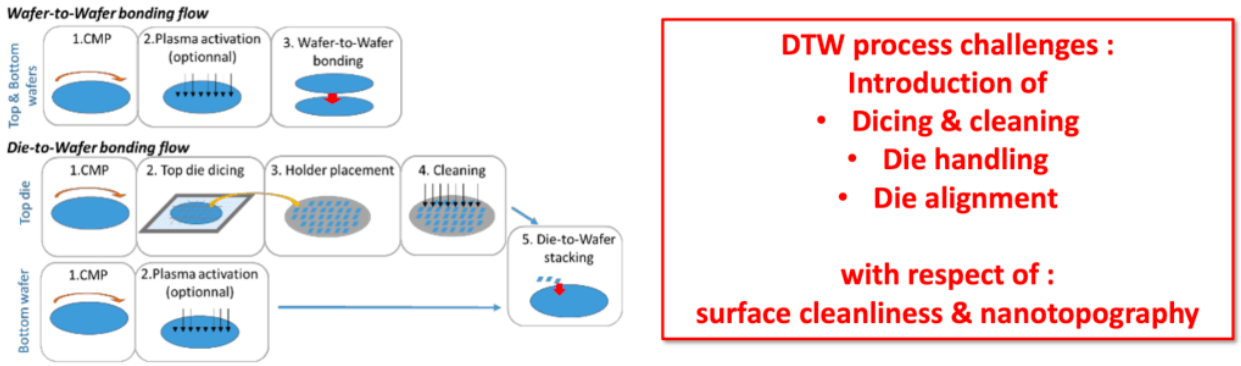

Fig. 2: Die-to-wafer, wafer-to-wafer hybrid bonding flows. Source: Source: Leti

SE: What else is involved with copper hybrid bonding?

Uhrmann: Besides clean processing of the dies without any yield loss from particles, a further challenge that is often underestimated is testing of dies and known good die (KGD) concepts. While bumped dies

can be tested, the hybrid bond structure is only a couple of micrometers in size and has extremely high surface quality, which does not allow for any electrical testing. Therefore, hybrid bonding is driving a lot of indirect testing processes in order to guarantee high-yielding chiplet systems. This is a steadily increasing challenge, where today we are talking about a couple of dies per system. The vision for the future is the partitioning of SoCs (system-on-a-chip) at an earlier metal level, hence, driving the needs of accuracy, cleanliness, planarization and fill processes to a new dimension.

SE: That's not the only challenge in packaging. Today, the semiconductor industry is in the midst of a boom cycle. In recent times, we've seen acute shortages of today's package types amid growing demand. We've also seen shortages in the packaging ecosystem, such as substrates. How can the industry deal with that?

Liu: In the past several months, I have observed an interesting phenomenon, given the shortage of laminate substrates. OSATs have come up with creative ways to work around the problem. I will give you two examples. One concerns QFN packaging. In the past, we always used laminate substrates to build flip-chip CSPs or flip-chip BGAs, which usually facilitate relatively larger package body sizes or larger dies. Given the shortage of laminate substrates over the past six months or so, JCET has figured out practical ways to produce larger QFNs with larger lead-frame footprints and finer pad pitches in order to satisfy the customer's demand for larger body sizes or IC dies. This is also readily acknowledging a lower number of I/Os compared to that of a true laminate. The other example pertains to fan-out packaging. Again, due to the substrate shortage, customers who wanted flip-chip BGAs or larger flip-chip CSPs would say, 'We can't get IC substrates anymore. What can we do?' As they couldn't work with QFN packages either, they would then start talking to our fan-out packaging engineers. They would ask if we could enlarge a given 10 x 10 millimeter fan-out or eWLB package to say 15 x 15. In doing so, we were indeed able to emulate what our customers were trying to achieve with a flip-chip CSP or BGA by means of a fan-out package. Fan-out doesn't need a laminate substrate, but rather a silicon base to provide support. In summary, material shortages have indeed propelled us industry practitioners to come up with fairly innovative engineering solutions in order to provide customers with the best possible products in a timely manner.

https://semiengineering.com/challenges-with-chiplets-and-packaging/