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Fan-Out And Packaging Challenges – October 6, 2021

Experts at the Table: Wafer-level and panel-level approaches, packaging economics, and the need for new materials.

Semiconductor Engineering sat down to discuss various IC packaging technologies, wafer-level and panel-level approaches, and the need for new materials with William Chen, a fellow at ASE; Michael Kelly, vice president of advanced packaging development and integration at Amkor; Richard Otte, president and CEO of Promex, the parent company of QP Technologies; Michael Liu, senior director of global technical marketing at JCET; and Thomas Uhrmann, director of business development at EV Group. What follows are excerpts of that conversation. To view part one of this discussion, click here. Part two is here.

SE: Fan-out is an advanced package type used by Apple and others to assemble one or more dies in an advanced package, enabling chips with better performance and more I/Os for applications like computing, IoT, networking and smartphones. Where does fan-out packaging fit today, and where is it going?

Chen: Fan-out started as a packaging innovation to extend the I/O footprint of wafer-level chip-scale packages (WLCSPs), while protecting the four sides from crack damage. The first high-volume product was known as eWLB (embedded wafer-level ball grid array). A competing version is Deca Technologies' M-Series fan-out. Together, they represent an important high-volume miniaturized package type for smartphones and other mobile applications. We are also thinking about fan-out technology for high-density and high-performance applications. The expansion of the fan-out concept of precise positioning of multiple die on carriers, reconstituting them into a wafer-like package format, followed by layers of redistribution circuitry is an important development in the advanced packaging landscape. From the menu perspective, it provides a rich continuum of packaging technologies from flip-chip BGA to the 2.5D silicon interposer application space, including emerging silicon bridges. We have a vibrant area of innovation and creativity serving the all-important areas of high-performance computing, AI, machine learning, and more.

Liu: What we're seeing is that the die-to-package ratio has been greatly improved with the latest fan-out wafer-level packages. We've also seen a steadily increasing demand for larger-size die fan-out packages. Moreover, we've received a number of new inquiries regarding TSV-less, chip-last types of fan-out packaging solutions. Interestingly, some of these fan-out SiP (system-in-package) inquiries pertain to ADAS and in-vehicle networking for automotive, rather than server, AI, 5G, or other high-performance computing applications.

Kelly: Fan-out and RDL (redistribution layer), in general, are large application spaces. People call a lot of different things fan-out. You can have fan-out packages with simpler single metal layers. That is one market case with its own growth curve. As you think about heterogeneous chiplets, and perhaps high-performance computing, you're talking about higher density, higher layer count fan-out products. Those have a place, as well. That dielectric is electrically a lot better than silicon oxynitride that you find in a 2.5D interposer. So if you have high-speed die-to-die interfaces, you may not be able to use a silicon interposer. Silicon interposers are great for HBM (high-bandwidth memory). That data bus doesn't run as fast. If you need faster interfaces, which engineers are coming up with all the time, the polyimide dielectric is better suited electrically. If you think about the supply chain, OSATs and foundries alike are working on their own RDL high-density fan-out type of constructions. So you don't have to have a special fab to create a silicon interposer. The supply chain is broader in high-density fan-out.

SE: High-density fan-out incorporates several chips in the same package, including HBM. Traditionally, HBM was mainly found in 2.5D packaging technologies. Will fan-out replace 2.5D?

Kelly: It's complementary to 2.5D and other packaging types. Everything isn't going into high-density fan-out, but certain pieces — especially chiplets — fit nicely. As the economics of 5nm and 3nm bear out, you need to minimize the use of the newest silicon nodes in your own product or it's not affordable. High-density fan-out RDL technologies have a place to enable that to happen.

SE: In the fan-out process flow, dies are placed in a round wafer-like structure. The dies are processed and then diced, resulting in individual fan-out packages. Meanwhile, in panel-level fan-out, the processes take place on a large square panel. A square panel can process more packages than a round wafer, which reduces the cost. Will panel-level fan-out ever become a mainstream technology? Any issues here?

Uhrmann: From our perspective right now, it's definitely a very hot topic. We are seeing a lot of investment here. It's the bridge, in my perspective, between PCB and some packages that can be done in fan-out. It's a bit of a threat to the PCB world. It would be the first time that you see fine line and space patterning slightly below 2µm on a panel. That's the interesting part where panel fan-out is going. Is that going high volume? That's a very good question. You need a high-volume driver in order to populate the panels and to make it worthwhile. But given how many panel lines are established in the world, we will see volumes for one application or another. For example, RF is something that's a good application for panel, where classical single-die fan-out processing is done, leaving out the complexity of multi-chip packages with high silicon cost.

Chen: The concept of panel-level fan-out is an extension of wafer-level fan-out, and its productivity advantages are obvious. Panel-level development and implementation depend significantly on the availability of special panel equipment capabilities, appropriate materials, and manufacturing processes. Close collaboration and partnership among users and tool and material suppliers are crucial. Currently, there are many variations in panel sizes, processes, and materials among the various contenders vying within this packaging space. What is often overlooked is that there must be sufficient volume of a fan-out product for panel fan-out to be justified. Today, there are limited cases with sufficient volume to support multiple suppliers. As fan-out moves to the larger sizes of advanced packages, such as AI and chiplet configurations, then panel fan-out becomes more easily justified.

Liu: This is a technology area that has a sizable growth potential, but there are still challenges, ranging from equipment/material readiness to production-proven yield control. Nevertheless, we're keeping a close eye on it.

SE: Are there any other issues here?

Otte: The major benefit from both fan-out wafer-level and panel-level packaging is cost reduction, largely through reduced labor cost, as material cost per device is similar to conventional packaging. Both of these processes are likely to be used primarily for high-volume devices where the last penny counts. If you asked about wafer-level packaging versus fan-out wafer-level packaging, I would have a different answer. We see an increasing number of sub-assemblies utilizing wafer-level assembly, with two approaches emerging. The first is fabricating a standard CMOS 12-inch wafer and then building on the individual sites on that wafer, attaching lids to accommodate fluids, mounting optical chains, as well as MEMS components and antennas. Then, you singulate the resulting structures. This combines the data gathering and processing power of electronics with non-electronic components used in sensors and I/O devices. The second trend we see is wafer-to-wafer bonding. Instead of placing individual parts on the sites on a wafer, a second wafer is bonded to the first, combining many sites in one step, thus reducing unit cost. That second wafer may be primarily silicon, glass or some alternative. In both of these cases, one objective is to reduce the cost by processing panels (arrays) to reduce handling.

SE: What's needed to accelerate momentum in packaging?

Otte: Better materials are really a great help in packaging. The industry is lagging in the development of new materials and their applications in real devices. Liquid crystal polymers, for example, have really good properties generally, but especially for RF devices. Yet we have not developed techniques to capitalized on them. Polyimide is not ideal because its properties vary significantly with water content that changes with the environment. The sources of substrates are also limited, and we have issues with sourcing molding compounds and adhesives. Currently, the various shortages illustrate that this is a real key issue. Then, we simply have too much concentration with suppliers in a volatile part of the world. We also don't carry enough inventory. We've taken the just-in-time concept too far. It's simply not going to work any longer as it is resulting in major costs, so we are going to see major changes. The situation is exacerbated because we have some real problems shaping up in Asia, including increasing tensions between China and the United States.

Liu: There are a few areas we need to focus on. Number one is the connection—in terms of R&D collaboration and technology sharing—between foundries and OSATs. This is fairly obvious. Neither camp could guarantee continual success without the other's support. This is especially true as the leading edge of die-to-die interconnect technology migrates from microbumps to hybrid bonding and eventually to direct copper bonding. Secondly, on the industry level, I would like to see more investments in critical components and materials, especially the ones essential to manufacturing chiplet/2.5D/3D packages. This is referring to our prior value-chain discussion. As an interdependent community, we all need to communicate with each other from time to time, instead of doing everything by ourselves behind closed doors. As an OSAT, JCET Group has been tracking LCP for some time now, and we'd welcome LCP material specialists and suppliers to continue sharing the latest product insights and solutions with us. LCP means liquid crystal polymer. As a material candidate with superior thermal stability, extremely low water absorption, stable dielectric constant (Dk) and loss tangent (Df) within high-frequency ranges, LCP has long been deemed a practical solution for making MMIC substrates, as well as MSL-1-ready package enclosures, such as LCP plastic lids processed with B-stage epoxy for achieving so-called 'near-hermetic' seals.

Chen: Packaging is gaining importance and momentum across all markets and applications. The packaging community has always understood the importance of working with fabless, foundries, and IDM communities, as well as with the system houses. With the rapid evolution towards heterogeneous integration and system-in-package, this need for collaboration across the industry boundaries has never been stronger. A very good example is the growing importance of chiplets in the waning days of lower digit nodes. How can we have chiplets and SiP engaging with sub-nanometer devices? We need to keep this momentum going. Packaging is playing an increasingly vital role. I am sure that the packaging community will take up this call.

Kelly: Customers look to OSATs for volume production. That's where customers come when they need to scale up their production. It's important for companies to invest in approaches that are compatible across several different product platforms so those expensive assets can be used wisely and to keep the costs relatively low. In the long term, we need to think about this concept for chiplets. There needs to be a compromise between customers and manufacturers, one that meets the functional needs and doesn't push the capital investments into niches. This must stay compatible across a broad swath so that we can keep costs relatively lower. Also, I would add that we need an incremental breakthrough in power generation and keeping total dissipated power in check. Power density per unit of area in silicon continues to go up. The more content you pack into a heterogeneous package, the more difficult and expensive the power challenge becomes.

Uhrmann: There's still a couple of years ahead for future scaling. People are smart here. They have this goal of following Moore's Law for years and ages. The IRDS International Roadmap for Devices and Systems is laid out beyond 2030. It's an important thing. It's there for the front-end. It's also there for equipment suppliers. When it comes to equipment, it can't be developed in half a year. When you need a

new breakthrough, the equipment needs to be developed, tested, put in place and qualified. Then, you can finally run it in production. It's just one piece in your whole manufacturing chain. So, the IRDS roadmap is great for equipment suppliers to achieve some of their targets. That is also triggering new technologies that are coming up on the space. That's triggering new materials that are needed at this insertion point. Now, let's look at chiplets and heterogeneous integration. You need to have something that runs in parallel to the IRDS roadmap. You also need the equipment, materials and everything here. We need to make sure all of these developments are ready.

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