semiconductor packaging news

Silicon Austria Labs and EV Group Collaborate in Optical Technology Research - November 16,

semiconductor packaging news

We search for industry news, so you don't need to.

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November 16, 2023

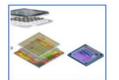
Eliminate the need for

operators to assess bond

testing failure modes at the

What Can Go Wrong In Heterogeneous Integration

The article discusses the challenges and potential pitfalls in heterogeneous integration, a critical aspect of advanced semiconductor technology. It highlights the complex nature of combining diverse materials, processes, and technologies in a single chip, emphasizing the need for precise planning ... Semiconductor Engineering



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to process the test result images. xyztec

DIE Stacking on a Small Area Assembly process where chips

are stacked on top of one another on a substrate. This vertical integration allows a compact arrangement of different circuits

with different dimensions on a small area.

Tresky Automation

Press Releases

Global Semiconductor Manufacturing Industry Set for Q4 2023 Recovery, SEMI Reports

The global semiconductor manufacturing industry is poised for a robust recovery in the fourth quarter of ...

Critical Cleaning Requirements to Overcome Advanced Packaging and

Defluxing Challenges As technology advances, wafer-level packages have emerged in many different varieties. Computing has evolved significantly over the years.

Technical Paper

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SUMMARY

Collaborate in Optical Technology Research

Silicon Austria Labs and EV Group

EV Group (EVG) and Silicon Austria Labs (SAL) announced that SAL has received and installed multiple EVG lithography and resist processing systems at its MicroFab R&D ...

Microsoft announces custom AI chip that could compete with Nvidia

Microsoft has unveiled its latest advancements in artificial intelligence hardware, introducing the Maia AI processor and ...

SUMMARY

CNBC

- **Technical Papers** Revising 5G RF Calibration Procedures For RF IC Production Testing
- Optimizing New Power Switch Technology Using Compound Semiconductors
- Targeted Sample Preparation for Deeply Buried ROI in Advanced Packages
- How AiP/AoP Technology Helps Enable 5G And More
- Decapsulation of Multi-Tier Wire-Bonded Semiconductors
- Series B: Adhesion and Bondibility of Al2O3-coated Bonding Wire
- How to Select RF Test Socket

UC-2210M - Urethane for Electronic

Component Protection epoxySet introduces a new and unique, urethane

potting compound. The UC-2210M was formulated to protect electronic components in high moisture and thermal ..

EpoxySet Inc.

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Advanced Component Labs, Inc.

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Sustainability 101: A Closer Look at E-waste

This article examines the pressing issue of electronic waste (e-waste). It delves into the environmental and \dots

3DInCites

Banned US chipmaking equipment still ending up in China

China's chipmaking ambitions face a setback as the US imposes stricter export controls on critical semiconductor ...

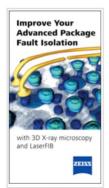
The Register

Huawei's 5G chip breakthrough needs a reality check

Huawei, the Chinese tech giant, has unveiled its latest 5G smartphone despite ongoing sanctions from the \dots

MIT Technology Review







SUMMARY

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SUMMARY

India's Wearable Market Grew 29.2% YoY to 48.1 Million Units, Says IDC

India's wearable market is on a roll, as the International Data Corporation (IDC) reports a stellar \dots

TDC

<u>Imec unveils a publicly accessible 'virtual fab' in an effort to realize net zero in chip fabrication</u>

IMEC, a leading research and innovation hub in nanoelectronics and digital technologies, has announced ambitious plans \dots

Digitimes

Chip inventory of Samsung, SK hynix remains high in Q3

Samsung Electronics and SK hynix have reported high semiconductor inventories in the third quarter of this ...

The Korea Times

Essential Inspection Requirements in the Era of Convergence

Herein, learn ways to optimize processes and boost quality as advanced packages and board assembly converge. Read more.



Koh Young America, Inc.

Die Bonding Pattern Recognition

Learn the challenges of vision processing and pattern recognition for die bonding and a state-of-the-art technology that uses radar referencing,

synthetic models, and active feedback.

Palomar Technologies, Inc.

TSMC founder in US for APEC meet

Morris Chang, the founder of Taiwan Semiconductor Manufacturing Co (TSMC), has arrived in San Francisco to \dots

Taipei Times





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Ouote of the Day

"If I have seen farther than other men, it is because I stood on the shoulders of giants." Sir Isaac Newton

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represents ASE's next generation of 3D heterogeneous integration architecture. ASE

The day was Nov 16. What year was it? Pizarro Traps Incan Emperor

Francisco Pizarro, the Spanish explorer and conquistador, springs a trap on the Incan emperor, Atahualoa.



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Cartoon of the Day











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Calendar

- Nov 16, 2023: Advanced Semiconductor Technology Conference (ASTC) 2023 November
- Dec 7, 2023: SiC—Silicon Carbide Webinar Series
- Dec 13, 2023: SEMICON Japan 2023
- Jan 7, 2024: ISS 2024—Industry Strategy Symposium

Essential Inspection Requirements

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Koh Young America, Inc.

Die Bonding Pattern Recognition

Learn the challenges of vision processing and pattern recognition for die bonding and a state-of-the-art technology that uses radar referencing, synthetic models, and active feedback. Palomar Technologies, Inc.

Test Your Knowledge Answer

What three South American countries does the equator cross?

Answer: Brazil, Colombia, Ecuador

What Year Was It Answer

Pizarro Traps Incan Emperor Answer: November 16, 1532

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