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EVG completes construction of Manufacturing V building – November 28, 2023

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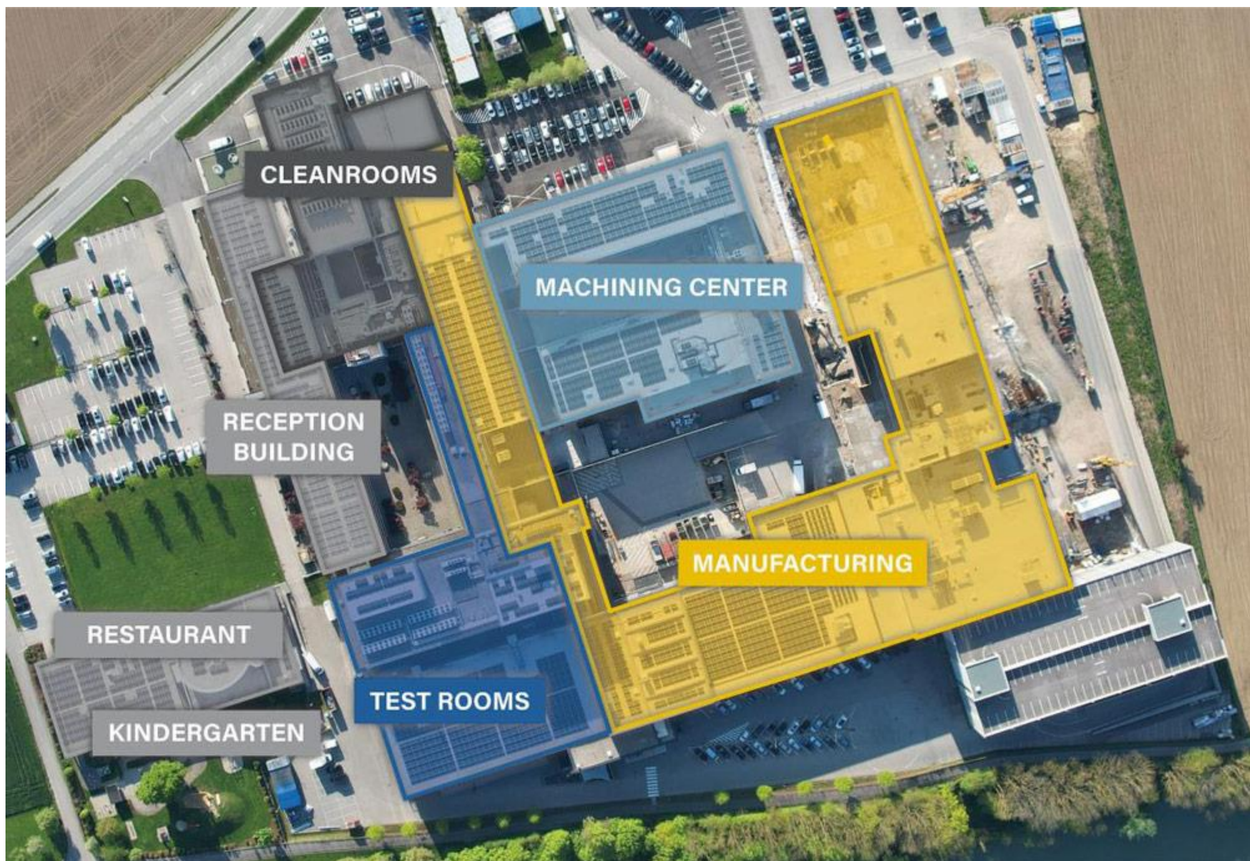
EV Group of St Florian, Austria – a supplier of wafer bonding and lithography equipment for semiconductor, micro-electro-mechanical systems (MEMS) and nanotechnology applications – has completed construction work for the next expansion phase of its corporate headquarters. The new 'Manufacturing V' facility, which is now open and serves as the manufacturing department for EVG equipment components, provides a significant increase in production floor and warehouse space.

The opening of the Manufacturing V facility is the latest in a series of expansion phases and investments driven by continued strong demand for EVG's hybrid bonding and other process solutions and process development services to support the rapidly growing advanced packaging and 3D/heterogeneous integration market.

Picture: Aerial view of EVG's corporate HQ in St. Florian, Austria. In the foreground are the completed Manufacturing IV and V buildings, as well as the Manufacturing VI building, which is under construction. Source: EVG.

The Manufacturing V facility adds more than 1200m2 of additional production floor space (for a total of more than 8100m2 of production area) and more than 1200m2 of warehouse space. Two new floors of office space have also been added above the manufacturing floor. In parallel, the existing Manufacturing II building was converted to offer nine new test rooms for the final assembly & test of EVG's high-precision systems, as well as for technical source inspection of the systems by customers. This has resulted in a 30% increase in test room area, bringing the total test room space at EVG's headquarters to nearly 2800m2.



Picture: Overhead view of EVG's corporate HQ. Source: EVG.

The opening of the Manufacturing V facility follows the company's previous expansion phase, Manufacturing IV (completed at the end of last year), which itself added nearly 1800m2 of production space and additional warehouse space. Since embarking on these two most recent growth phases, EVG has expanded its production capacity by more than 60%.

Manufacturing VI, EVG's next phase of expansion that provides for an additional 1400m2 of production and an equal amount of warehouse space, is already under construction, with completion scheduled for second-half 2024.

"New applications fueling the semiconductor industry, such as AI, high-performance computing and autonomous driving, require massive innovations in advanced packaging," says Dr Werner Thallner, executive operations & financial director and member of the executive board. "As key process enablers for 3D/heterogeneous integration, fusion and hybrid bonding have been transformed into the new scaling mechanism for semiconductor manufacturing. EVG is at the forefront in developing fusion and hybrid bonding and other process solutions that our customers need to support their current and future capacity ramps as well as their long-term product roadmaps," he adds. "The growth in demand for our products over the years has led us to make major investments in expanding EVG's manufacturing and cleanroom capacity to meet our customers' evolving needs. We fully expect this demand growth to continue in the years ahead."

Heterogeneous integration solutions

EVG's wafer bonding, lithography and metrology solutions enable the development and high-volume manufacturing of technology innovations in advanced packaging — including backside-illuminated CMOS image sensors and other 3D-IC stacked devices — as well as in MEMS and compound semiconductors. Recent breakthroughs in hybrid bonding to address the needs for 3D device integration, wafer bond alignment technology to address future 3D-IC packaging requirements, IR laser release technology to eliminate glass substrates for advanced packaging and enable thin-layer 3D stacking, maskless exposure for fan-out wafer-level packaging (FOWLP), and nanoimprint lithography NIL and resist processing to support wafer-level optics (WLO) manufacturing, are just a few examples of EVG's technology for heterogeneous integration and wafer-level packaging.

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