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Dr. Michael Töpper, IZM: "We stand at the forefront in packaging!" - November 10, 2021

Dr. Michael Töpper, Fraunhofer IZM: "We are already holding initial talks about transferring to a commercial panel level packaging line." IZM and panel level packaging

Panel Level Packaging promises a significant reduction in the cost of ICs. In an interview, Dr. Michael Töpper, Business Development at the Fraunhofer Institute for Reliability and Microintegration, explains what other advantages PLP brings and how the PLP Consortium 2.0 is driving development.

Markt&Technik: The Panel Level Packaging Consortium 2.0 (PLC 2.0) is in the second year of its two-and-a-half-year duration. Why is this new packaging technology at panel level so promising?

Dr. Michael Töpper: For a number of reasons: Firstly, manufacturing on the large panels promises to reduce costs by about 30 percent compared to the wafer level. Among other things, this is because a lot of material is saved because there is much less waste: Hardly any material is lost on the rectangular panels. Secondly, this improves the CO2 balance and points the way toward CO2-neutral semiconductor manufacturing – another important factor. We have already created an initial model that can be used to estimate the CO2 footprint of the panel-level packaging process. This will enable consortium members to identify the energy-intensive phases of the process and optimize it.

What is special about the project from your point of view?

The fact that very different manufacturers from the ecosystem surrounding panel level packaging can coordinate with each other, from material manufacturers such as BASF and Ajinomoto to manufacturers of the placement machines, the lithography systems, and manufacturers of sputtering and electroplating systems. Only if everyone works closely together can the many challenges be mastered.

For example, the different expansion coefficients of silicon and the plastic material?

This is a major difficulty that we have already been able to solve. The dies are placed on the substrate by the placement machines – in our case with machines from ASM – and then sealed with the molding compound. Then the molding compound is cured in a temperature step. This causes the dies to shift slightly from their original location; more so, the further they are located along the edge.

We measured this “die shift” optically in detail to know how far the dies shift depending on their position on the panel. Once that is known, the placement machines can be set to place the dies offset by exactly that amount. As a result, when the panel is cured, they end up exactly where they are supposed to be. Then the lithography process can proceed smoothly, and the fine-line redistribution layer can be structured over the entire area of the panel with the required accuracy. To achieve this, manufacturers of the materials, manufacturers of the placement machines and manufacturers of the lithography machines must communicate closely with each other.

Another challenge is that, during the measurement process, huge amounts of data are generated, which must be evaluated so that the corrected positioning data can then be made available to the placement machines.

What lithography technology is used?

We rely on laser direct imaging; in our line we use lithography equipment of the German company Schmoll. This company is known as a specialist for drilling printed circuit boards and now wants to penetrate this market.

Manufacturers of the machines required for panel level packaging come from quite different sectors.

Yes, because panel level packaging is where different technologies come together. In the past, the laser direct writers we use were mainly used for PCB production and were considered rather slow with very high optical resolution. That is no longer the case; their processing speed has increased greatly, as has their flexibility. But there are also lithography companies that come from wafer manufacturing such as EVG and Süss.

In addition, many manufacturers of machines for LCD manufacturing are now turning their attention to this topic. The cards are being reshuffled among manufacturers who have previously focused on equipment for wafer processing, for PCB manufacturing and for LCD panel manufacturing.

One of the next process steps is sputtering. Are there any problems here?

Again, the organic material proves to be much less simple than known from the almost ideal substrate silicon. The organic matrix absorbs moisture, which should be disposed of before the sputtering process would trap it. Then there would be damage. But we can also solve this problem.

What other essential process steps are required?

Electroplating is very important – here we work together with Atotec, Semsysco and Rena. In addition, of course, we must not forget analytics and measurement technology.

This all sounds like a substantial investment to be able to install the panel level packaging line in the first place ...

... which we were able to do thanks to investments made by the German Federal Ministry of Education and Research to promote the Research Fab Microelectronics Germany. This enabled us to install the new equipment during the run-up to the PLC 2.0 project.

The die shift in panels has already been mentioned. Another difficulty is that the panels warp – again caused by the different expansion coefficients – during the process steps due to the different temperatures at which they operate. What can be done about this?

This is also a major focus of PLC 2.0. In this area, we are working with companies in the field of debonding. For example, the company ERS in Germering near Munich has developed such a debonding machine, which cools the panel evenly over its entire surface and thus counteracts warpage very effectively. By the way, being able to precisely control the temperature curve of the panel is also very important when placing the dies with the position data, in which the die shift is already taken into account, so that ERS's technology can also be used here.

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