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By Hesham Taha [Teramount Ltd] and Martin Eibelhuber [EV Group]

Silicon photonics has emerged as a promising platform for supporting the ever-growing demand for high-speed data transfer, low-power consumption and low latency, which are required for the next generations of data centers, advanced computing, and 5G/6G networks and sensors. The silicon photonics market has expanded significantly in the last few years and is expected to grow at a 26.8% compound annual growth rate (CAGR) over the next five years [1]. While wafer manufacturing capabilities for silicon photonics are well advanced through the use of standard semiconductor mass-production processes and existing infrastructure, silicon photonics packaging and testing are still behind and lack production scalability, which limits wider deployment of silicon photonics. Photonic Bump technology, a new wafer-level implementation of optical elements for scalable packaging and testing capabilities, is presented in this article. The Photonic Bump is an equivalent of electrical solder bumps and has the potential to align silicon photonics with standard semiconductor wafer manufacturing and packaging lines, thereby bridging the gap in silicon photonics toward high-volume manufacturing.

Fiber-to-chip assembly is the main limiting factor in existing silicon photonics packaging solutions, which use direct fiber bonding on a photonic chip with adhesives through active alignment or specialized high-precision alignment equipment. These are limited in their volume manufacturability, scalability to large numbers of fibers, compatibility with packaging processes such as reflow requirements, and integration with electronics packaging. The essence of the problem is related to geometrical constraints of tight assembly tolerances when packaging single-mode fibers with silicon or nitride waveguide channels on a photonic chip, as well as related to the complex side-coupling geometry. These impose critical obstacles for silicon photonics to be able to be applied to wider applications such as co-packaged optics in ethernet switches, advanced computing and future chip-to-chip optical connectivity.

Teramount and EV Group have collaborated to adopt wafer-level optics technologies in order to enhance silicon photonics packaging processes. Under this collaboration, nanoimprint lithography (NIL) has been used for wafer-level implementation of Photonic Bumps on silicon photonics wafers.

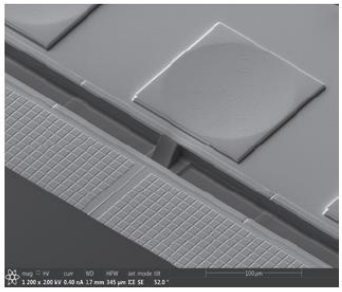

Figure 1: Photonic Bump wafer-level imprint on a silicon photonics wafer at accurate placement relative to waveguide channel.

Photonic Bump elements provide unique optical coupling functionalities that include: 1) a vertical beam deflection to enable wide-band surface coupling as a replacement for the complicated side-coupling geometry; and 2) a spot size conversion for mode matching between single-mode fiber and the chip's waveguide (see **Figure 1**). In addition, Photonic Bumps are used to enable the "self-aligning optics" scheme when connected with the Teramount PhotonicPlug fiber connector [2], which enables fiber-chip assembly tolerances of larger than ±20µm/1dB (see **Figure 2**).

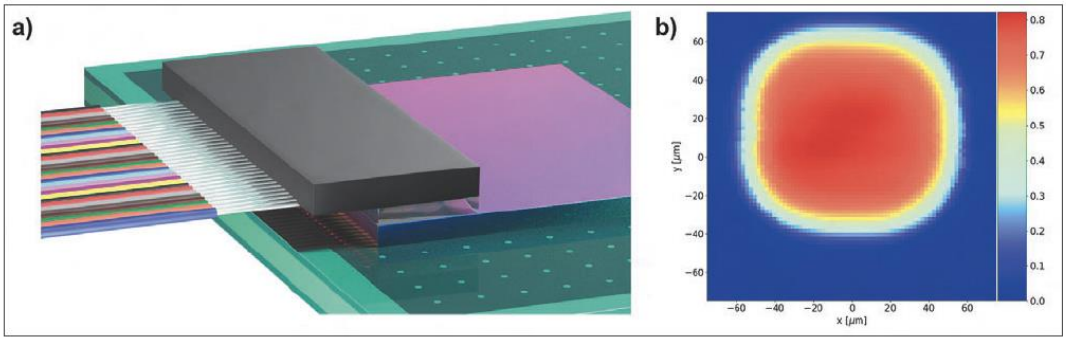

Figure 2: a) (left): PhotonicPlug assembled on a photonic "bumped" silicon photonic chip. b) (right): Measured XY fiber-chip tolerance providing larger than 100 times of fiber-chip assembly tolerance compared with existing technologies.

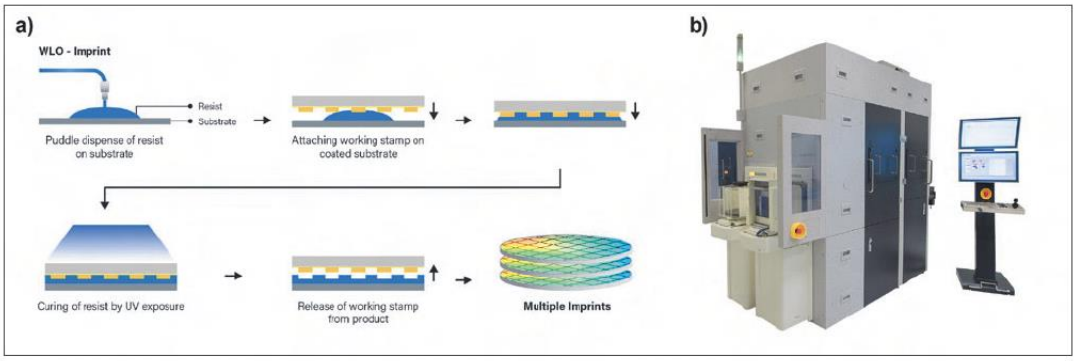

Figure 3: a) (left) Typical process flow for imprinting wafer-level optics, which can be accomplished by b) (right) an EVG7300 UV nanoimprint lithography system. The EVG7300 UV-NIL system can support multiple processes, including SmartNIL, wafer-level optics and device stacking.

The combination of large assembly tolerances and wide-band surface coupling enables the transition of silicon photonics packaging from specialized equipment to standard passive alignment assembly protocols and tools. This transition supports high-yield and high-volume packaging. In addition, it allows unique packaging protocols such as detachable and post-reflow fiber connectivity, which are optimized for assemblies with large numbers of fibers and co-packaged optics applications. Moreover, the PhotonicPlug and the Photonic Bump, fueled with their surface coupling and large tolerances, create an effective wafer-level testing capability prior to wafer dicing, thereby enhancing silicon photonics wafer manufacturing yields.

Application of NIL to silicon photonics

NIL has proven to be the most effective method of replicating complex structures, such as 2.5D features, grayscale patterns and freeform optics, because it is not limited to the constraints of optical lithography. Standard optical lithography is optimized to build up structures layer by layer. While this layer by layer approach makes it ideally suited to the needs of the electronics industry, it is not sufficient for manufacturing photonic structures. In contrast, NIL enables the patterning of 3D structures in a single-step process, which is ideally suited for the photonics industry where light-matter interaction relies largely on shape and geometry [3]. For example, NIL allows the imprint of complex geometries such as sharp edges of deflector mirrors, curved surfaces, high and low aspect ratio structures as well as imprinting in deep cavities. Wafer-level optics (WLO) processes have long proven their high repeatability in high-volume production for optical sensors and are now being leveraged for photonic packaging.

The NIL process offers significant yield and cost advantages for the above-mentioned structures compared to conventional manufacturing methods, such as diamond drilling, laser direct writing and electron-beam writing, which have very low throughput and are therefore difficult to scale up to larger substrates and volume-production environments. Incorporating the NIL process enables the use of best-performing dies and the ability to efficiently bring these high-quality patterns into production lines.

Teramount worked with EVG to establish suitable manufacturing process solutions for Teramount's Photonic Bump. In the development work, a wafer-scale master stamp with the Photonic Bump structures was produced from a single-die "hard master" using EVG's Step and Repeat (S&R) NIL process. This scaling enables wafer-level mass-production processes, and is typically based on two steps. First, the S&R master is used to replicate multiple working stamps. Next, the working stamps are used to imprint the functional photonic structures on the target substrates (see **Figure 3**). While multiple replications are needed to support the scaling and to avoid wear out of the single die master, the final imprints of the fully-functional optical structures demonstrated high pattern fidelity, precise alignment and precise control of desired layer thicknesses. Scanning electron microscope (SEM) inspection showed residual layer thickness at <1% of the structure height and high alignment accuracy to within less than 500nm. In particular, the precise alignment to the optical structures underneath the photonic chip is crucial for the excellent coupling performance described above.

Working in conjunction with the Photonic Bump packaging technology, NIL is now making wafer-scale packaging possible in the photonics industry, which could have a profound impact on lowering packaging and overall product costs. Whereas packaging is still a relatively small (but growing) share of overall complementary metal-oxide semiconductor (CMOS) production costs, it represents the majority of overall cost in photonics manufacturing, which still relies on single-device packaging schemes. Wafer-level integrated photonics, enabled by NIL and Photonic Bump packaging, has the potential to flip this equation.

The ability of NIL to provide accurate placement of optical elements on silicon photonics wafers plays a critical role in shifting the typical fiber packaging

complexity from the assembly domain to the wafer manufacturing domain. It provides an ideal platform for post-processing of silicon photonic wafers for the photonic "bumping" process to be performed either at semiconductor foundries, or at outsourced semiconductor assembly and test (OSAT) facilities. As part of the joint collaboration, EVG provided NIL process development and prototyping services through its NILPhotonics Competence Center, as well as expertise in both CMOS and photonics manufacturing, to assist Teramount in accelerating the development and productization of its PhotonicPlug technology.

Summary

The Photonic Bump is a transformational solution for establishing a scalable silicon photonics packaging platform that generates, for the first time, an effective "through-chip optical via" for seamless photonics and electronics integration through 3D packaging and interposer geometries. It holds the promise to align silicon photonics with the standard semiconductor manufacturing ecosystem and to leverage silicon photonics to volume manufacturing for a variety of emerging applications.

References

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Biographies

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