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ECTC Highlights Next-Generation Packaging Challenges - June 29, 2022

Large crowds mulled the latest substrate trends and new developments in 3-D IC hybrid bonding.

The IEEE Electronics Components and Technology Conference (ECTC) returned to an in-person conference at the end of May with more than 1,500 attendees, domestic and international. Attendance in San Diego matched pre-pandemic numbers. While some presentations remained virtual, using video recording, many were onsite. A variety of electronics packaging topics were discussed. Judging by the crowded rooms, this year's hot topic was 3-D IC hybrid bonding.

Advanced packaging. A pre-conference Heterogeneous Integration Roadmap workshop discussed trends in networking for the future and new developments in advanced packaging for high-performance computing and data centers. The workshop concluded with a panel of presenters discussing the latest trends in medical health and wearables.

Plenary sessions covered some of the latest topics. The MicroLED display session focused on high-volume manufacturing progress and challenges. In a session on the evolution of IC substrate technology, panelists from Intel, Amkor, Ajinomoto, AT&S and Atotech discussed the latest substrate trends.

The special session – Meeting Next Generation Packaging Challenges from Chiplets to Co-packaged Optics – included panelists from AMD, Cisco, Marvell and Synopsys (FIGURE 1). Panelists discussed the importance of co-design and changing the approach to design, including system-level design. The combination of digital and photonics is coming. Integrating this in 3-D will include the laser, modulator, filters and detectors. Interfaces and the design platform are important for robust manufacturing, including product quality, debug and traceability, and in-field optimization. The panel concluded that, with increased use of chiplets, continued work is required in the areas of test and known good die (KGD), thermals, power deliver and system-level integrity. Adoption of standards such as the recently introduced UCIe is important to align the industry around an open platform to enable chiplet-based solutions. Thermal management remains one of the major bottlenecks with 3-D.

FIGURE 1. A special panel on packaging challenges. Panelists included (from left) Kevin O'Buckley (Marvell), Raja Swaminathan (AMD), Ming Zhang (Synopsys), Ravi Mahajan (Intel), Sandeep Razdan (Cisco Systems), and moderator Jan Vardaman (TechSearch).

A special night session focused on the US Department of Defense (DoD) in the state-of-the-art heterogeneous integration (SHIP) program. The opening statement from the office of the Undersecretary of Defense for Research and Engineering explained the backdrop of the program. Speakers from Intel and Qorvo, recipients of US government funding, described their activities. Qorvo is focused on RF, and Intel is focused on high-performance computing with its embedded multi-die bridge (EMIB) technology. The panel admitted that, in the absence of a volume supplier of buildup substrates, the DoD depends on a global substrate procurement strategy.

A session on diversity and career growth provided advice from a panel of experts, including representatives from IBM, Lam Research, Edwards and Cadence. The plenary session covered digital transformation with participation from Intel, TSMC, Yole, Onto Innovation and Samsung. A late-night session focused on Interconnect Technologies for Chiplets with participants from Intel, IBM, Unimicron, TSMC, SPIL and Furukawa Electric. Participants from Taiwan and Japan dialed into the session to discuss topics including embedded bridge, the incorporation of memory in advanced package developments in optical packaging, 3-D packaging and substrates.

Adapting to substrate shortages. With the continued substrate shortage, companies focused on the potential for a fan-out wafer level package (FO-WLP). Numerous presentations covered several options, with new applications for fan-out discussed. SK Hynix discussed the potential for memory applications. IME A*Star discussed FO-WLP antenna-in-package (AiP) for automotive radar applications. Researchers at UCLA described their work on FO for micro displays. RFcore discussed FO-AiP for 5G mmWave applications. Amkor, ASE and Samsung presented package options for FO-WLP.

Processing FO in a panel has been proposed as a way to lower the cost by increasing the number of parts with large-area processing. Fraunhofer and the Technical University of Berlin discussed the technology limits of panel processing, describing warpage and die shift as the major issues. Layout adaptation is promoted to overcome die-shift challenges on large panels. Samsung Electronics discussed the reliability of the via structure in its FOPLP line. Amkor introduced its 650mm x 650mm panel line. Nepes provided reliability data on FO packages fabricated on its new panel line based on Deca M-Series technology (FIGURE 2). Deca Technologies described 20µm device pad pitch with its M-Series process. The use of adaptive patterning provides a way to handle die shift. Dai Nippon Printing introduced its panel-based RDL interposer with a 2µm pitch semi-adaptive process for chiplet integration.

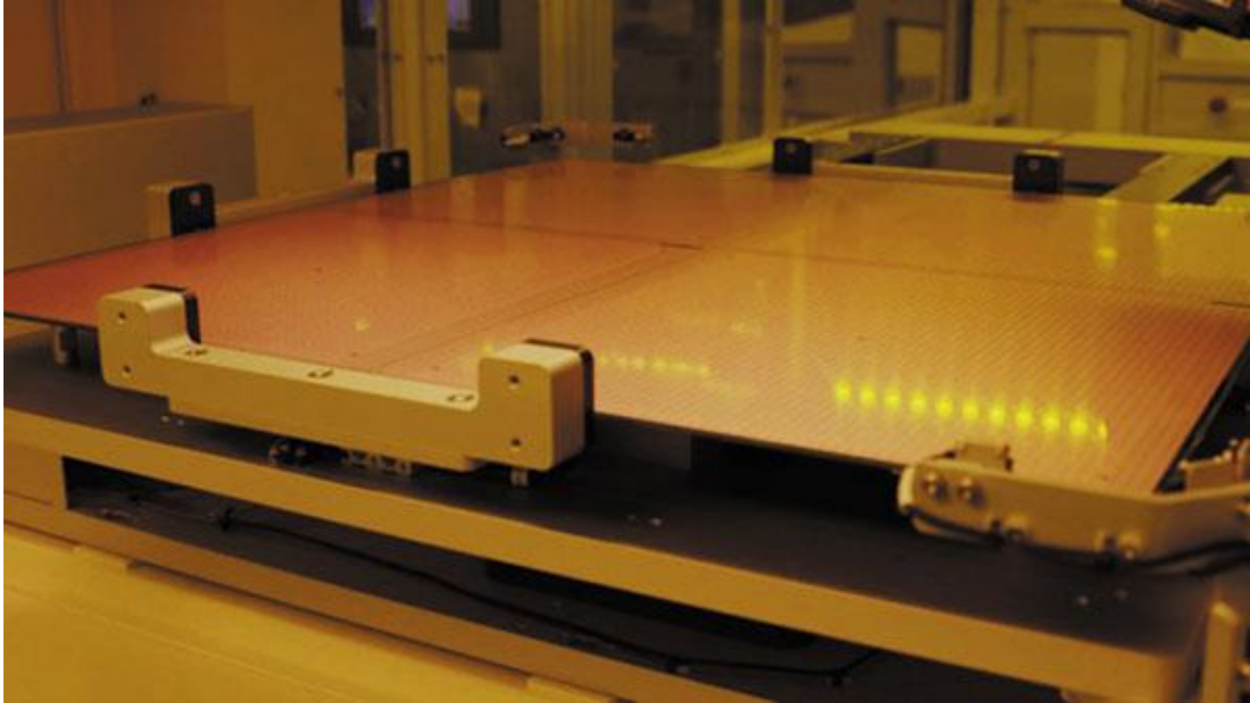

FIGURE 2. The Nepes nPLP 600mm x 600mm fanout panel line reportedly can produce five times as many chips as one 300mm round panel.

Several presentations focused on new substrate options, including glass as a substrate and RDL interposers. Developments in glass substrates were introduced with papers from Korea Electronics Technology Institute and Georgia Tech. TSMC introduced its organic interposer CoWoS-R+ technology that replaces the silicon interposer with an RDL structure. The plus indicates the integration of a large amount of high-density integrated passive devices (IPDs) that serve as decoupling capacitors. The integrated de-cap capacitors suppress the power domain noise and enhance HBM3 signal integrity at a high data rate. Optional silicon connection blocks (bridges) provide high-density die-to-die connections. IBM provided updated work on its direct bonded heterogeneous integration (DBHi) silicon-bridge package, in which the Si bridge is connected to the die and then mounted on the laminate substrate. SPIL provided recent reliability data for its embedded bridge package. Unimicron discussed its hybrid substrate with a buildup film.

3-D hybrid bonding. Three years ago, many ECTC papers focused on R&D activities in hybrid bonding. This year, more than 30 papers discussed hybrid bonding process improvements and new developments. While image sensors have been using hybrid bonding for many years, Sony described their recent work to develop 1µm face-to-face bonding and a new thinning process that minimizes Si thickness variation across the wafer. Adeia's (formerly Xperi) study of the influence of Cu microstructure on the thermal budget shows the possibility of a 20° to 40° reduction in the final anneal temperature. CEA-Leti presented research conducted with Intel on a new die-to-wafer (D2W) collective bonding self-assembly process using water droplets with high alignment accuracy and high throughput. SK Hynix reported the work on wafer-to-wafer (W2S) DRAM stacking for DRAM. Samsung presented several papers on hybrid bonding, including research on controlling bonding voids. AMD described its V-Cache, now in commercial production for servers, desktops and gaming, using TSMC's SoIC process. TSMC described an extension of its SoIC process.

Co-packaged optics. Several presentations focused on co-packaged optics (CPO). Rockley Photonics introduced a fan-out silicon photonics module for next-generation CPO. Rain Tree and IME A*STAR described a heterogeneous integration package using FO-WLP for a hyperscale data center. IBM Canada, GlobalFoundries and others discussed optical fiber pigtail integration for CPO. Cisco described its vision for CPO and challenges in the use of through-silicon vias, including high warpage, optical fiber

coupling, and chip-on-substrate assembly. Reliability requirements were also highlighted. A joint paper from EV Group, Tyndall National Institute, IMEC and Ghent University described a high-speed Si photonic switch with a micro-transfer-printed III-V amplifier. ASE described its CPO assembly.

Emerging areas. Presentations also covered additive manufacturing, 3-D printing, developments in packaging and assembly for wearables, and micro LEDs.

Next year's ECTC will be held in Orlando May 30 to Jun. 2.

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https://www.pcdandf.com/pcdesign/index.php/current-issue/234-forefront/16638-ectc-highlights-next-generation-packaging-challenges