



**EV Group Earns Outstanding 10th Consecutive Triple Crown Win in TechInsights 2022 Customer Satisfaction Survey - June 17, 2022**



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### Semiconductor Industry R&D is Alive and Well

The decline of centralized semiconductor industry R&D labs, as well as the technical challenges facing semiconductor manufacturers, have helped the rise of independent research and development institutions. These organizations such as imec and CEA-LETI, both in Europe, are funded in part by local and regional governments, but more importantly, they are funded by companies either performing pre-competitive research with the R&D centers as the primary project manager, or companies that choose to use imec or Leti as an extension of their research centers and use the R&D centers resources in addition to those of their own.

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IFTLE 523: What is the #1 Wafer-level Fan-out Technology In Production?

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Sustainability 101: The Struggle to Remove Lead from Solders

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**ADVANCED SYSTEM IN PACKAGE TECHNOLOGY**  
CONFERENCE & EXHIBITION

June 21-23, 2022  
DoubleTree by Hilton Sonoma - Wine Country

### What's Happening at the IMAPS SiP Conference?

Combining the 3D ASiP and IMAPS SiP events into an all-in-one comprehensive program, IMAPS established the Advanced System-in-Package conference to focus exclusively on innovative SiP technology developments, solutions and business trends.

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## I am Manufacturing 1: Intro to Manufacturing Top of Form

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## Conversations from the Technology Corner at ECTC 2022

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### Member of the Week

# cādence®

Cadence is a leader in electronic systems design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent system design strategy to deliver software, hardware, and IP that turn design concepts into reality. With extensive advanced packaging experience, Cadence offers a comprehensive 3D-IC design solution to address the requirements for digital SoCs, analog/mixed-signal designs, and entire systems. The comprehensive solution spans integration, packaging, custom and digital implementation, verification, system analysis, and interconnect IP for chiplet-based designs, including system design of advanced packaging, safe and secure embedded software, and PCBs; analysis of electromagnetic and electrothermal effects of semiconductors, packages, boards, and systems; and co-optimization with semiconductor devices.

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## Community News

[Cadence Digital and Custom/Analog Design Flows Certified by TSMC for Latest N3E and N4P Processes](#)

[StratEdge Displays High-Performance Semiconductor Packages at IMS 2022, June 21-23, in Booth 4089](#)

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[Onto Announces New EB40 All-Surface Inspection Module for Wafer Fabs and Advanced Packaging](#)

Recommended Reads

[Ways To Address The Materials Crunch – SemiEngineering](#)

## Events

[IMAPS SiP Conference](#)

June 21-23

[FLEX Conference & Exhibition 2022](#)

July 11-14

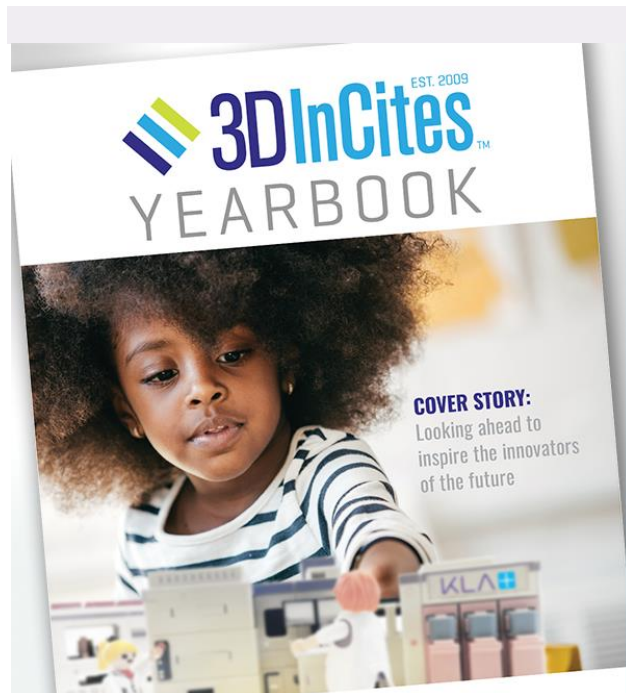
[SEMICON West HYBRID 2022](#)

July 11-14

[IEEE IEDM 2022 Call for Papers July 14 Deadline](#)

[9th ESTC \(Electronics System-Integration Technology Conference\)](#)

September 13-16



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