DAC/Semicon West Addresses Top Issues, Trends For Chips – July 12, 2023

Semiconductor

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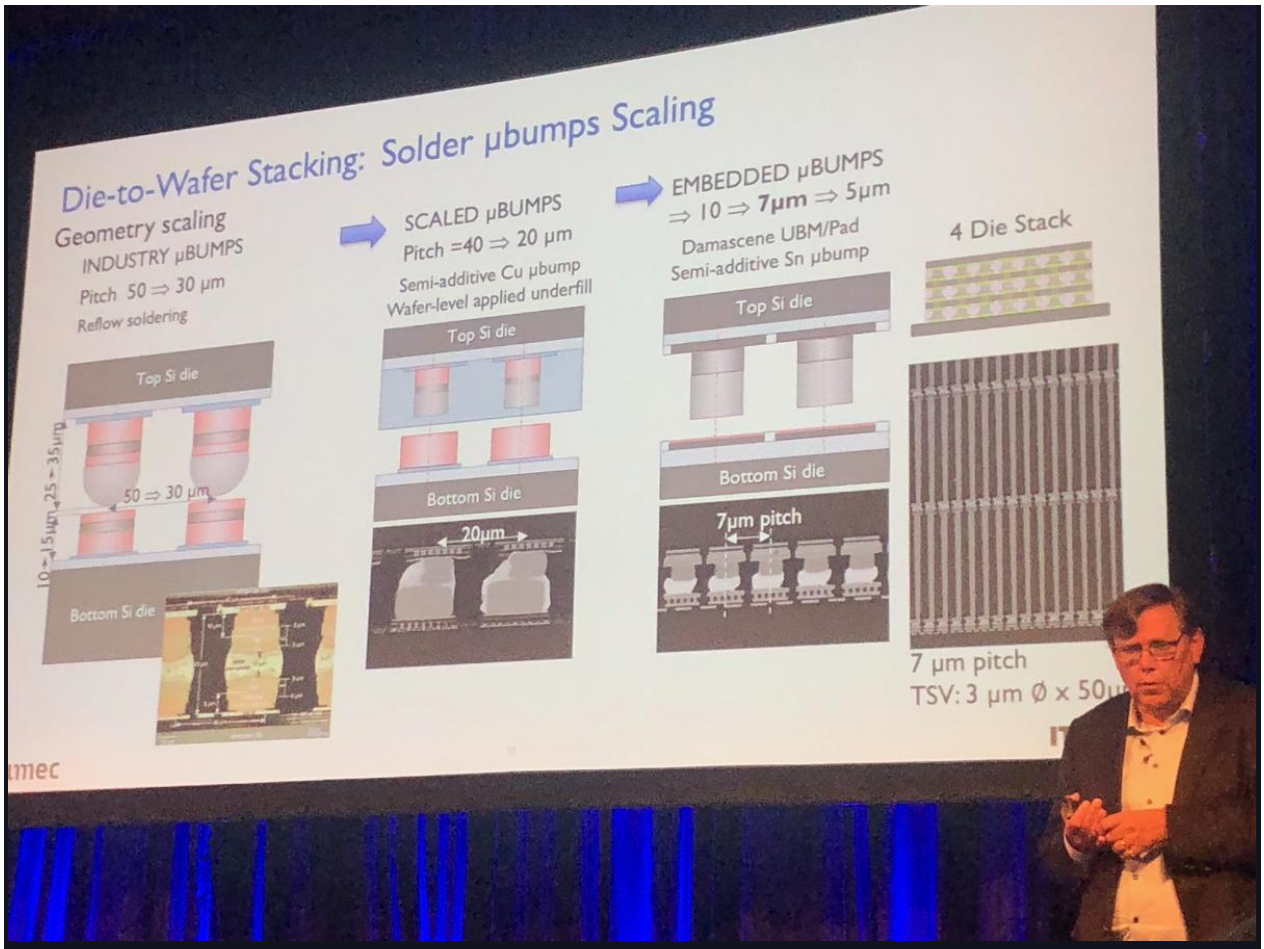
The Design Automation Conference (DAC) 2023 and Semicon West returned in full force this week, drawing in more attendees and sponsor companies than since before the pandemic. At times, booth traffic was four to five deep, blocking aisles, and standing room only was common at presentations.

Hot topics included generative AI and the underlying semiconductor technology, data security, reliability, automotive electronics and autonomous vehicles, and the overall need for AI/ML to process more data more quickly in order to reduce costs and time to market.

Imec roadmap highlights drivers in packaging

At Semicon West, **imec** reiterated the industry's commitment to extending Moore's law with EUV and high NA EUV, while highlighting advanced packaging's latest developments. The parallel approach to leading-edge advancement, will accelerate roadmaps though reliance on industry collaboration. Eric Beyne, senior fellow at imec emphasized the various solutions for advanced packaging that enable reduced RC delay and optimized performance — from hybrid bonding to backside power delivery — thermocompression bonding to C4 bumps. Technology demand for performance and cost of manufacturing continue to be interdependent.


Die-to-Wafer Stacking: Solder µbumps Scaling
Geometry scaling
INDUSTRY µBUMPS
Pitch 50 ⇒ 30 µm
Reflow soldering
Top Si die
50 ⇒ 30 µm
10 ⇒ 15µm 25 ⇒ 35µm
Bottom Si die
SCALED µBUMPS
Pitch =40 ⇒ 20 µm
Semi-additive Cu µbump
Wafer-level applied underfill
Top Si die
Bottom Si die
20µm
EMBEDDED µBUMPS
⇒ 10 ⇒ 7µm ⇒ 5µm
Damascene UBM/Pad
Semi-additive Sn µbump
Top Si die
Bottom Si die
7µm pitch
4 Die Stack
7 µm pitch
TSV: 3 µm Ø x 50
imec

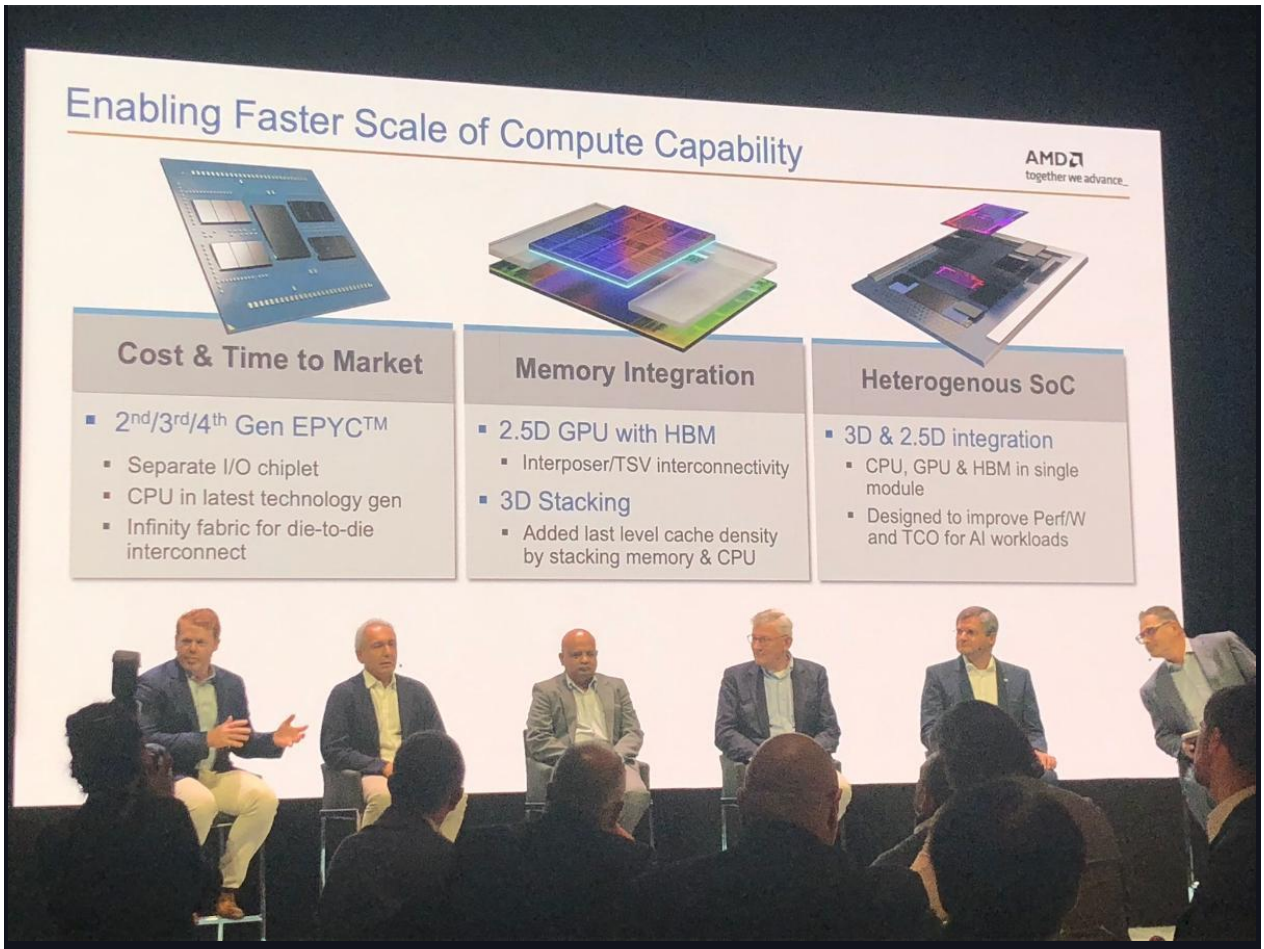


Eric Beyne, senior fellow at imec, outlines pivotal changes in hybrid bonding and bump technology. Source: Semiconductor Engineering / Laura Peters

System-level Integration, hybrid bonding are enablers

At **Applied Materials**' technology forum, the emphasis was on packaging approaches — from glass substrates to wafer-to-wafer hybrid bonding to optical interconnects. For perspective, wafer-to-wafer bonding could enjoy a lifetime that is comparable to wire bond interconnects once the process becomes robust. Glass substrates could start replacing interposers because they provide a more stable substrate. And system-level integration is becoming increasingly important for all applications.


Enabling Faster Scale of Compute Capability
AMD
together we advance_
Cost & Time to Market
2nd/3rd/4th Gen EPYC™
Separate I/O chiplet
CPU in latest technology gen
Infinity fabric for die-to-die interconnect
Memory Integration
2.5D GPU with HBM
Interposer/TSV interconnectivity
3D Stacking
Added last level cache density by stacking memory & CPU
Heterogenous SoC
3D & 2.5D integration
CPU, GPU & HBM in single module
Designed to improve Perf/W and TCO for AI workloads



Panelists discussed interconnect alternatives, glass substrates and hybrid bonding as key components enabling technology advancement. (left to right) Mark Fuselier, senior vice president of technology and product engineering at AMD; Babak Sabi, senior vice president and the general manager of Assembly & Test Technology Development (ATTD) at Intel; Chidi Chidambaram, Qualcomm fellow; Richard Blickman, president and CEO of BESI; Paul Lindner, executive technology director of EV Group; and Vincent DiCaprio, vice president, Semiconductor Products Group of Applied Materials. Source: Semiconductor Engineering / Laura Peters

Market Symposium

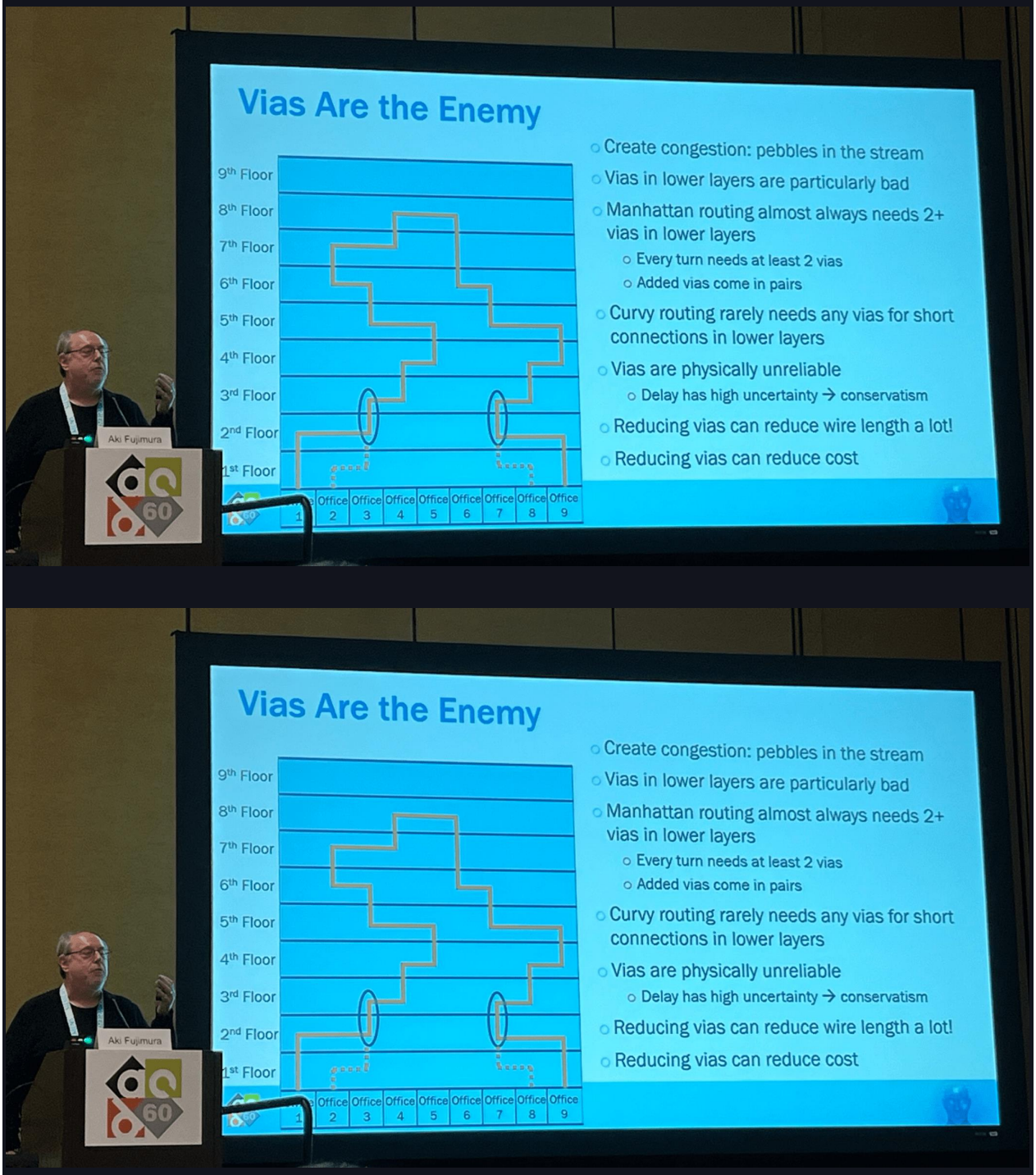
At Monday's SEMI Market Symposium speakers from manufacturers and investment/analyst companies weighed in on the state of the industry. Common themes included collaboration, certainty, agility, sustainability. They addressed the challenges and discussed solutions with respect to achieving simultaneous goals of achieving $1 trillion in revenue, lowering the carbon footprint and coping with the geographical shift of manufacturing operations. From the electronics manufacturing systems perspective, **Jabil**'s Dan Gamota noted that the distinct manufacturing roles of foundries, OSATs have begun to blur. Elias D Esadi, EY Parthenon, said the recent pandemic and the current geopolitical environment are prompting companies to build resilience into the supply chain. To do so companies are turning to more partnerships. And in his talk on packaging solutions for the growing automotive market, **Amkor Technology**'s Prasad Droned highlighted the diverse package types needed to support the ADAS and EV's power ICS. For instance, radar parts packaging has evolved to support antenna in package.

SEMI predicts strong rebound for semiconductor equipment
SEMI released its Mid-Year Total Semiconductor Equipment Forecast, predicting a strong rebound in global sales for 2024, following a steep drop in 2023 to $87.4 Billion, 18.6% below the record $107.4 Billion in 2022. SEMI forecasts $100 billion in global sales for 2024, driven by both front-end and back-end equipment.

LAM Research CEO Tim Archer discussed the potential of a $1 trillion market driven by AI and deep learning to improve design reliability, fault analysis, and supply chain reliability, and to shorten time to market.

Curvilinear manufacturing is now possible and is gaining interest for its potential to increase yield, reduce chip size, use less power, and increase performance and reliability. In a panel on Curvy Design, presenters discussed the advantages of curvilinear features, including the elimination of vias, improved layout efficiency, and greater process control. But its adoption faces will require changes for EDA software redesigns, organizational dynamics, and test and measurement.

Above, left to right, Steve Kieg , CEO Perceive; Andrew Kahng, professor at UCSD; Ezequiel Russell, senior director of mask technology, Micron; John Kibarian, CEO, PDF Solutions; Aki Fujimura, D2S (not pictured) at the Curvy Design Panel at DAC 2023.



Steve Keig, CEO of Perceive, explains why vias are not your friend, at the Curvy Design Panel, DAC 2023. Source: Semiconductor Engineering / Susan Rambo

Arizona State University (ASU) and **Applied Materials** announced plans to create the Materials-to-Fab (MTF) Research Center in ASU's Research Park.

Announcements

proteanTecs and **Teradyne** announced a strategic partnership to bring machine learning-driven telemetry to SoC testing that offers in-line, real-time performance enhanced monitoring of electronics based on deep data. The new process resides within an SoC running test software and providing telemetry that can detect a coming fault in a chip before a real fault is happening, so preventive measures can be take. "We believe the future of understanding how electronics perform in the field must be based on deep data," says Nir Sever, Senior Director of Business Development at proteanTecs.

Dutch company Nearfield Instruments announced an innovative new non-destructive, in-line metrology tool, AUDIRA, that provides measurements of subsurface features and identifies defects by combining acoustic force microscopy with atomic force microscopy to "listen" to sound waves coming through wafer layers. The new technology provides complementary metrology for in-line CD-SEM and TEM systems for subsurface process control measurements.

Flex Con keynotes

Keynote speakers from **META**, **Rice University**, and **Pragmatic Semiconductor** laid out some of the innovations and concerns with flexible electronics — and the semiconductor industry in general — at FLEX Con, SEMI's co-located flexible electronics conference. Among the highlights was a discussion about lightweight modular fabs that could be set up at a customer's site.

Richard Price, CTO of Pragmatic Semiconductor, holds up a strip of flexible electronics. Source: Semiconductor Engineering / Susan Rambo

Kris Erickson, research manager at **Meta Reality Labs**, went through advancements in AME (additively manufactured electronics), which are thin flexible electronics made through printing (screen, aerosol, inject, electro-hydrodynamic), powder bed fusion, fused deposition modeling (FDM), direct write (DW), stereolithography, and resin jetting. He stressed that each AME method has its strengths and weaknesses, making for a complexity of the choices.


FLEX
INTELLIGENTLY
FLEXIBLE

Kris Erickson, the research manager at Meta Reality Labs, talks about additively manufactured electronics (AME) at FLEX Con on Monday July 11, 2023. Source: Semiconductor Engineering / Susan Rambo

Michelle Michot Foss, a Rice University fellow in energy, minerals, and materials, is now working on carbon nanotubes at the Baker Institute at Rice University, pointed out that carbon on its own is not something you can or should ban. She asked where is the funding for carbon nanotube research and said the U.S. governmental bodies were still investing in the traditional mining industry. “And carbon-based products are actually the fastest growing of all materials out there. And why? Because metals are

inconvenient and they're heavy. They're useful for things like conducting electricity and stuff like that. But they're really problematic," said Foss. She explained that liquid hydrocarbons are easier to extract (compared with ore) and that it produces a lot of minerals used in many industries, but that being able to sell the fuel made the extraction of it monetarily viable. She did not think just extracting the minerals alone for semiconductors and EVs would be enough of a revenue stream for mining companies. She looked at how China was doing much of the smelting of gallium and germanium.

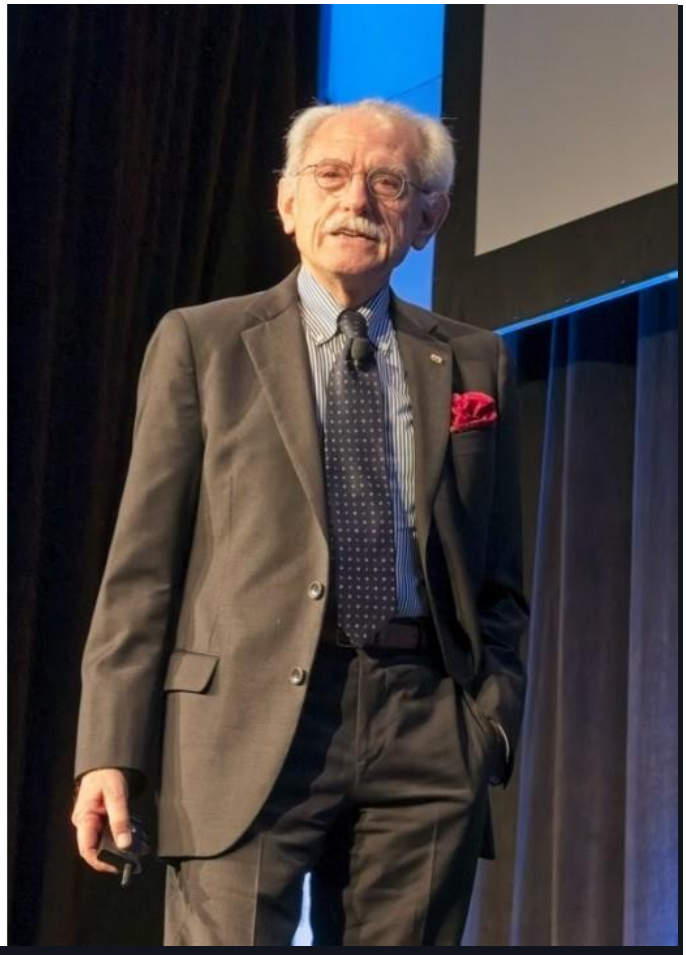
Michelle Micholt Foss, fellow in energy, minerals, and materials at Rice University, Baker Institute for Public Policy. Source: Semiconductor engineering / Susan Rambo

DAC news and highlights

Siemens' Mike Ellow looked at some recent impacts for semiconductors, from COVID to trade wars, AI. He also mentioned that society has started to demand more corporate responsibility about sustainability, and that implies that semiconductors are at the center of change. In addition, he said the world is becoming data-based, and projecting the amount of data that will be around in 2030 leads to staggering demands being placed on all parts of the industry. But while society depends on semiconductors, a large gap is developing involving the necessary talent.

Systems are becoming multi-domain and more connected. This impacts total complexity. Connections no longer can be in one direction. In the future, that will lead to catastrophic results. People need AI to make them more productive, something that will require more multi-domain virtual platforms that can be decomposed into implementation lanes.

He added that while digital twins have existed for a long time in some of the domains, they have not been connected, and that needs to change.



Above left, Mike Ellow, executive vice president, Electronic Design Automation Global Sales, Services and Customer Support at Siemens Digital Industries Software, spoke at the Design Automation Conference (DAC) in San Francisco on July 10, 2023. Above right, Alberto L Sangiovanni-Vincentelli, chair of electrical engineering and computer sciences, U.C. Berkeley, gave a keynote at DAC 2023 on Monday, July 10 in San Francisco, Calif. Source: Semiconductor Engineering / Jesse Allen

Of gods, heroes, and humans — DAC Keynote of U.C. Berkeley's Sangiovanni-Vincentelli
All Alberto L Sangiovanni-Vincentelli's talks start with a review of the past through classical art and architecture. Monday's DAC keynote, delivered by Sangiovanni-Vincentelli, the chair of electrical engineering and computer sciences at U.C. Berkeley, was no different, going from the age of gods, through the age of heroes where imaginative men take change, and then the age of men and reason. And then something new happens and you loop back through.

During the age of heroes, things like complexity are challenging, and so we constrain the degrees of freedom to make it easier to handle. Since 2000, we have had no new abstractions. There has only been incremental improvement.

The advent of 3D-IC is the big change. This is being driven by reticle limits, form factors required for new devices, and many other factors. But in the past integration on chip was the driver. This demands

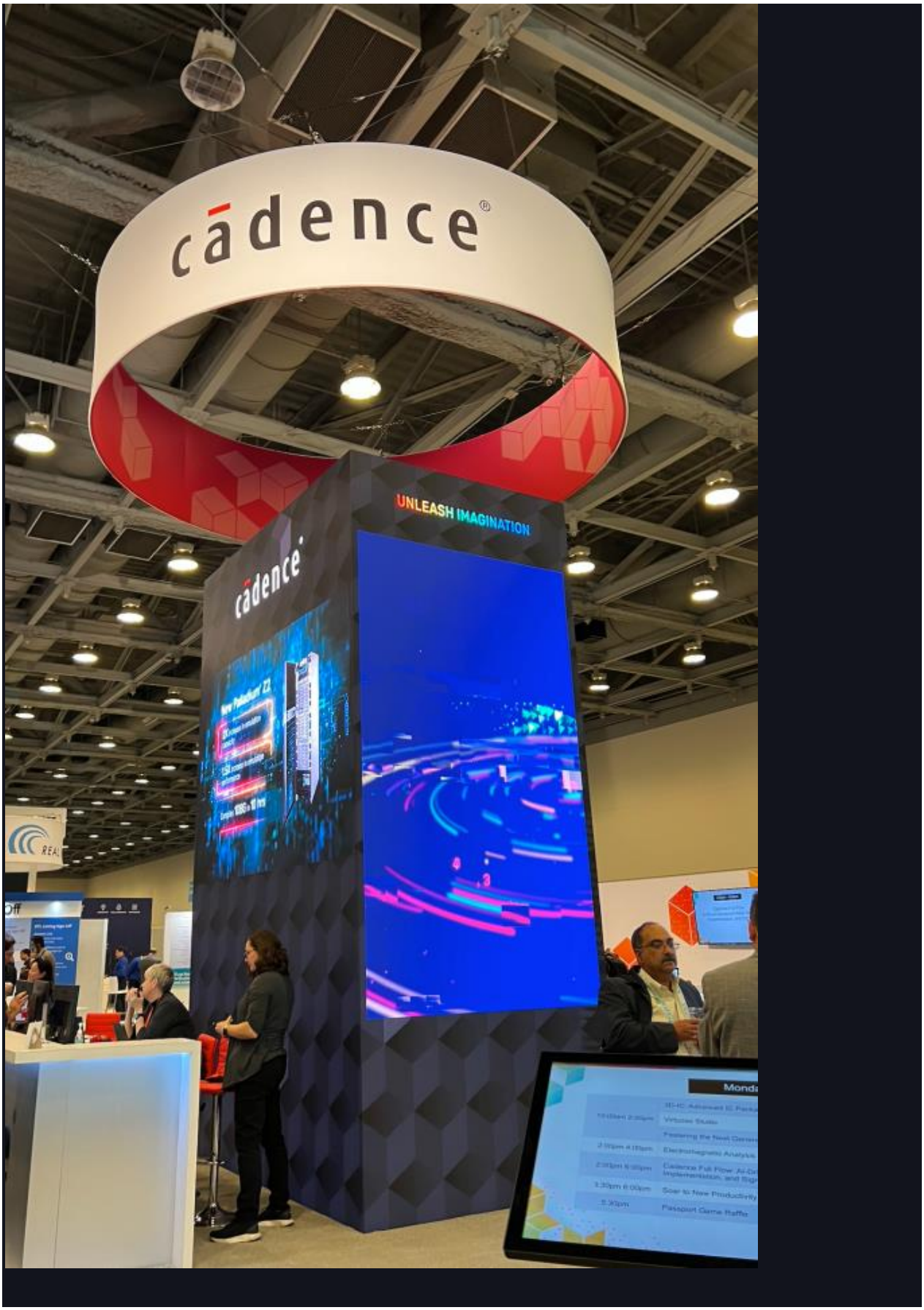
innovation in packaging. In the past 3D failed because 2D advances were so good. That has stopped being the case. We need to merge the people designing the chips with those doing the package.

This extends out to cyber-mechanical systems, and we need the platforms that can handle them. This requires multiple physics and different solvers for each of the abstractions. There are no common semantic domains across many of them.

Sangiovanni-Vincentelli also talked about the lack of talented people being created. Is AI a panacea? He outlined the impact of AI in DAC and said we have been doing AI for a long time according to the definitions. We need to insert a notion of sustainability in AI. Today there is an increasing amount of unstructured data. We are beginning to have computations that can handle that data. But it requires people to understand how to use the data with domain specific knowledge to make real advances. Within EDA, Alberto believes that the right way is to use AI to automate the flows. Tasks such as optimization and debugging are prime candidates.

In general, you have to combine physics with data and not just plug huge amounts of data into solving the problem. We need explainable AI that can also mitigate inherent bias.

Show floor images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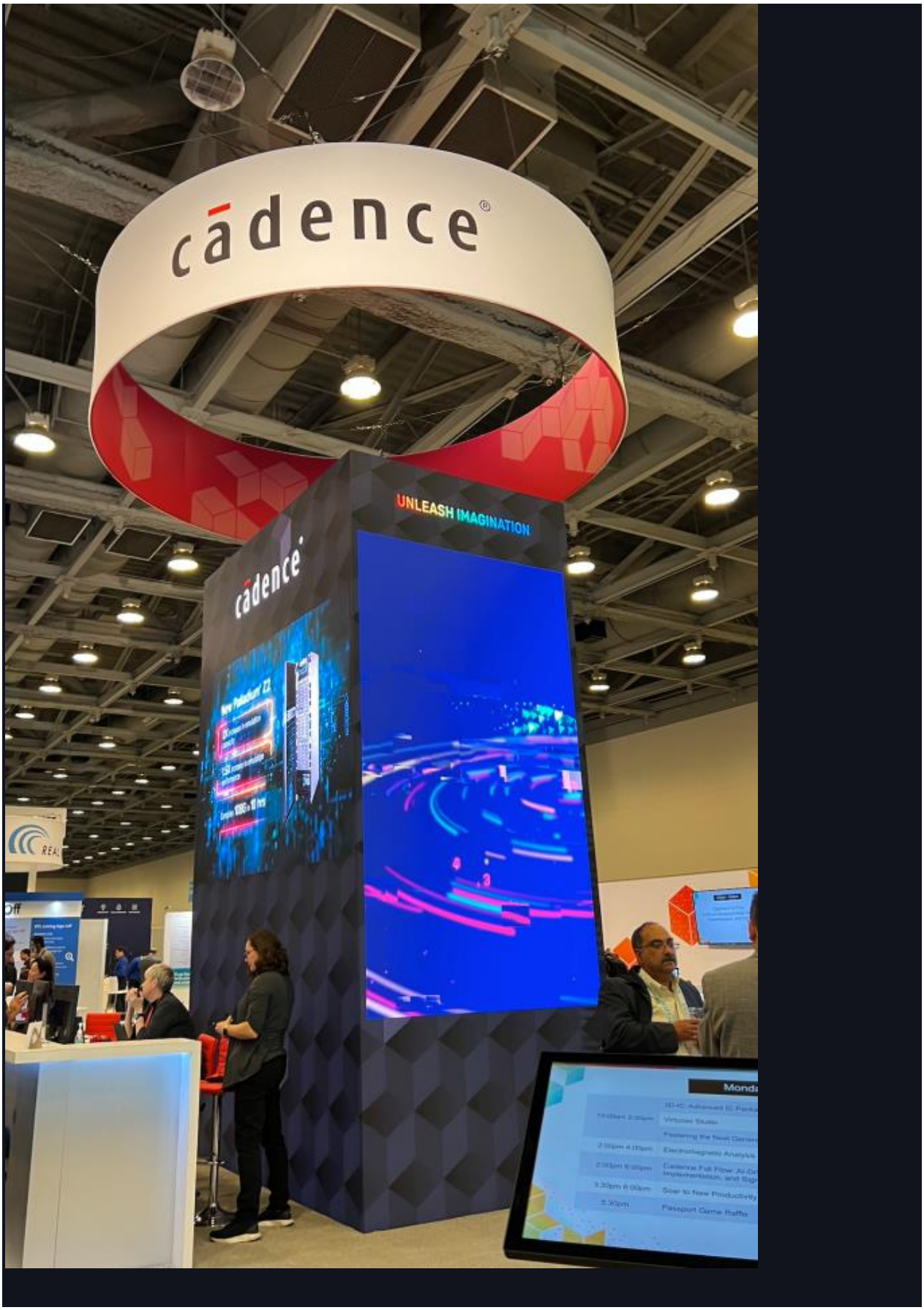
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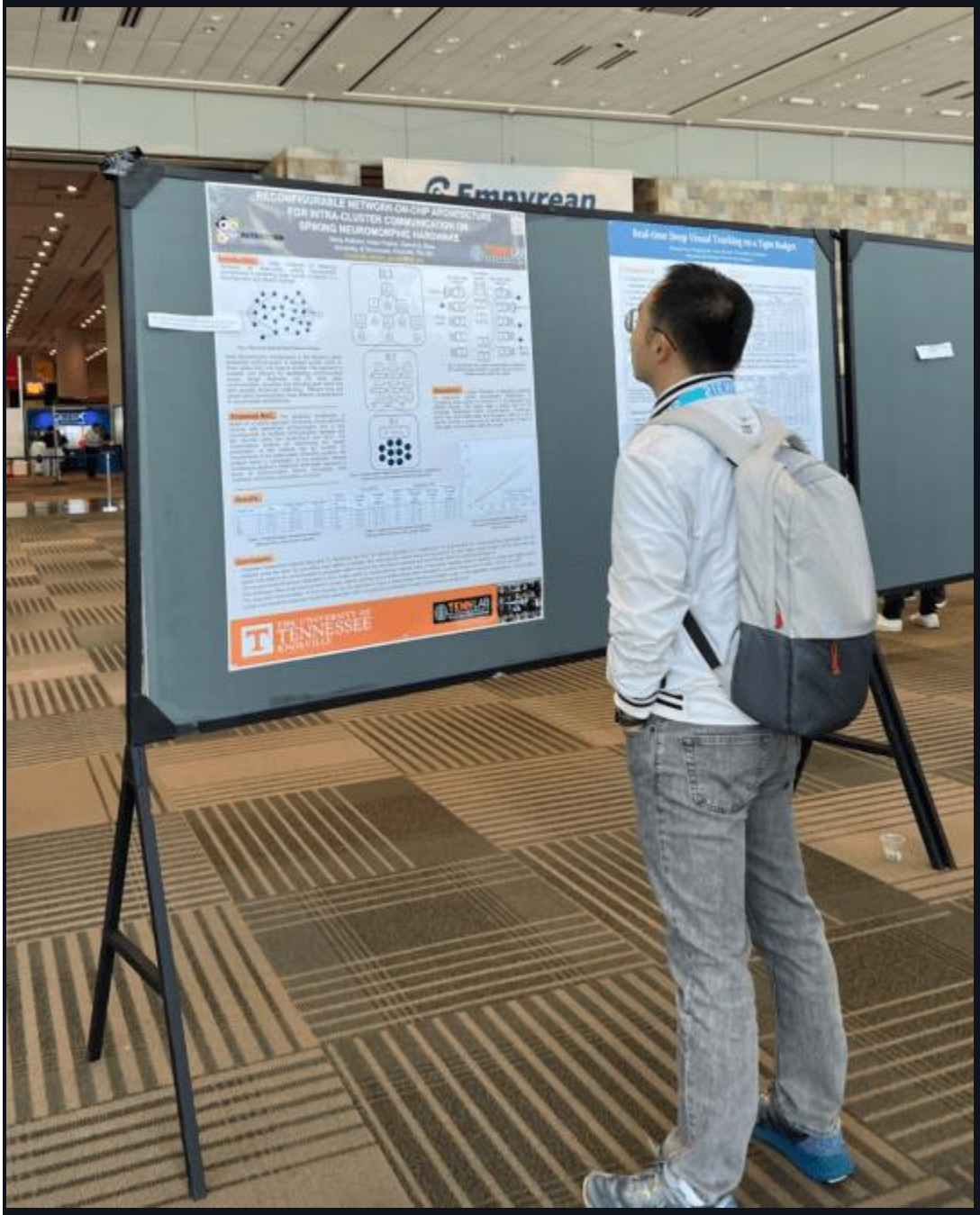
Cadence’s booth on the DAC 2023 expo floor. Source: Semiconductor Engineering /Susan Rambo



Reading research posters at DAC 2023.

- BlockOffsets. Modernizing Environmental Offset Ownership. Access Here.
- Source: https://semiengineering.com/dac-semicon-west-monday-and-tuesday-highlights/

https://zephyrnet.com/dac-semicon-west-addresses-top-issues-trends-for-chips/