PRINTED CIRCUIT DESIGN & FAB

Advanced Packaging: The Hot Topic in the Florida Sun – July 3, 2023

Advanced Packaging: The Hot Topic in the Florida Sun

Published: 03 July 2023
by Jan Vardaman

ECTC revealed the latest developments in 3-D hybrid bonding.

More than 50 presentations on hybrid bonding filled rooms to capacity at the IEEE Electronics Components and Technology Conference (ECTC) in Orlando, as did the Tuesday morning panel session. That panel discussion, on "Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications," organized by Infinera and Qualcomm and moderated by TechSearch International, included perspectives from design and EDA (Synopsys) and research institute IMEC, users of hybrid bonding (AMD with production at TSMC and Intel with its internal development program), equipment makers Besi and EVG, and yield and reliability specialist PDF Solutions.

Synopsys pointed out the importance of design tools and IMEC described key drivers for 2.5-D and 3-D integration technologies such as increasing system complexity, increasing need for heterogeneous integration, increasing die-to-die interconnect data bandwidth (more interconnect channels and higher interconnect speeds per interconnect), reducing die-to-die interconnect energy with shorter distance interconnect, scaled, lower capacitance interconnects, and lower voltage. IMEC noted the issue is not the number of interconnects but rather the available (local) interconnect density enabled by interconnect pitch scaling. Many of today's hybrid bonding applications using die-to-wafer structures are focused on the high-performance space where the cost can be justified, including stacking SRAM cache and logic-on-logic, as introduced by AMD's products in desktop, servers, and AI/machine learning.

Energy efficiency is driving development of new packaging solutions for the high-performance space. 3-D hybrid bonding offers more than three times the interconnect energy efficiency and more than 15 times the interconnect density compared to microbump solutions, according to AMD. 3-D hybrid bond interconnect is not without challenges, however, including external IP/die/package integration, new materials, power delivery, yield, test and cost, as described by Intel. While Besi and EVG presented options for the assembly, all agree that process yield depends on controlling particles and cleanliness. There was general agreement that die-to-wafer is more challenging than wafer-to-wafer. PDF reminded

the audience that despite the presenter lineup, reliability should not be the last consideration! Responses to audience questions made it clear that test and known good die are essential to the success of the technology. The race to introduce hybrid bonding for high bandwidth memory (HBM) was apparent in dueling papers from Samsung and SK Hynix, as well as updates on Micron's activities. TSMC also presented the potential for the use of hybrid bonding in photonics applications where the EIC and PIC could be stacked. Wafer-to-wafer stacking has been in products for many years for image sensors and MEMS, and Sony continues to report progress in wafer-to-wafer bonding with larger chips. Volumes are expected to increase for 3-D NAND flash where wafer-to-wafer bonding is used to stack layers, as evidenced by recent announcements from Western Digital and Kioxia for licensing Adeia's direct bond interconnect technology.

More hot panel topics. Panels and professional development courses before the start of the full conference were well attended. A panel on "Advanced Integration Roadmap for Harsh Environment – Current Status and Opportunities" led by Fraunhofer and Robert Bosch featured panelists from GM, Robert Bosch, ASE, Samsung, TSMC, Henkel, TU Delft, and Georgia Tech. TSMC suggested that with the large body sizes for ADAS, its CoWoS-R using an organic interposer instead of silicon interposer may be well suited to large-body-size packages. ASE explained that large packages often require board-level underfill, and corner balls are an issue for AEC-Q104. ASE reminded the audience that its FOCoS and FOCoS bridge packages reduce the pressure on substrates because routing in the RDL permits relaxed features and fewer build-up layers for the laminate substrate. Henkel noted requests for high-heat dissipation with underfill. Georgia Tech sees thermal (heat fluxes) as the biggest challenge.

A special session on "Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption," chaired by CEA-Leti and Cisco featured representatives from both organizations plus IBM, iNEMI, Teramount and Ficotec.

The Tuesday afternoon panel "Advanced Packaging Manufacturing in North America: Building the Ecosystem" was also a packed session. Organized by GE Research, ASE and TechSearch International, the panel featured representatives from government organizations (NIST and DARPA). DARPA's presentation explained the 3-D heterogeneous integration (3DHI) R&D focus areas such as multichip, multi-technology assembly and packaging (including die-to-die, wafer-to-wafer, die-to-wafer, and wafer-to-board processes, 3DHI interconnects (including fine-scale printing and additive manufacturing), thermal and power (including embedded thermal management with assembly and package, materials to extend temperature operation range, low-loss passive for power distribution, and efficient power conversion), tools for design, simulation and test, and prototyping services (including a 3-D assembly design kit).

The NIST presentation explained the purpose of the CHIPS for America bill is to strengthen and advance US leadership in R&D, developing an integrated ecosystem that drives innovation through a partnership with industry, academia, government and allies. A National Semiconductor Technology Center and a National Advanced Packaging Manufacturing Program will be created. The act is focused on significantly reducing the time and cost of moving from design to commercialization for member organizations and making semiconductor design capabilities accessible to a wide range of stakeholders. The program will establish and provide access to physical assets such as facilities, tools, and equipment with high capital costs. Access to in-house technical staff to assist with overcoming technical and process challenges will also be provided. Creating an investment fund that is structured to attract significant private capital into semiconductor-focused emerging companies is also part of the plan. Building a sustainable workforce is also emphasized as key.

Industry was represented by Marvell Technology, Micron and Promex (a small North American OSAT). Promex explained the difficulties for small companies to raise funds to match government incentives and asked the important question: Who will be the customer for US-based packaging services? Barriers to onshoring include the current limited onshore capability and higher cost of US domestic production. Benefits to onshoring include turn time, ability to visit, communicate and learn, confidentiality, and the availability of alternate sources. Promex suggested focusing investment on emerging and next generations of packaging, developing improved technologies, construction of pilot lines, demonstration of capability and performance, then establishing relationships and price. Micron indicated labor cost was not the main problem for onshoring, but rather everything else. Efficiency is important. Collaboration on equipment and materials is essential. In response to a question about workforce development, Marvell

indicated a need for technicians, adding that partnerships with community colleges are helpful. UCLA provided a university perspective, indicating the importance of working with industry and the role in education by providing a program that produces students with a multi-disciplinary background.

The Heterogeneous Integration Roadmap (HIR) Workshop, simultaneously held on Tuesday, included a perspective on Artificial Intelligence and Machine Learning in Package Co-Design for Chiplets, a discussion of challenges and opportunities for the heterogeneous integration of MEMs and sensors, an update on the US CHIPS and Science Act, and a presentation on additively manufactured electronics for heterogeneous integration.

Tuesday evening's panel discussion organized by IBM and Rapidus (Japan's new 2nm technology node silicon foundry) examined the Future of High-Density Substrates – Toward Submicron Technology. Presentations by Shinko Electric, Unimicron, Dai Nippon Printing (DNP), IBM and Penn State University highlighted the latest research on high-density substrate developments and glass packaging. Shinko Electric described its iTHOP high density organic interposer. Unimicron described challenges in producing large-area build-up substrates (>120mm x 120mm with more than 20 layers). New, semiconductor-like materials and equipment are required for future advanced substrates. Warpage control is essential. DNP described its work with a glass core substrate. IBM described its dual chip module (split die) and mentioned the importance of good test coverage. Penn State is working on glass with a focus on RF applications. Standards for chiplet design were discussed including Bunch of Wires (BoW), and Universal Chiplet Interconnect Express (UCIe), with the latter having more momentum.

The conference opened Wednesday with a keynote by Professor Michael J. Manfra of Purdue University on "Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging," in which he explained that advances in quantum hardware on multiple scales are required to reach the promise of quantum computing.

Wednesday night the panel chaired by Brewer Science and GE Research from ECTC coordinated with University of Toronto from ITherm, the co-located conference, focused on diversifying the technical workforce to meet national needs including CHIPS Act initiatives. Panel members included representatives from University of Texas, Arlington, NextFlex, GE Foundation, and NIST.

On Thursday the conference opened with a panel chaired by Metawave Corporation and Fraunhofer with a discussion on "Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems," including panel members from Teledyne Scientific, Northrop Grumman Space Systems, HRL Laboratories, Penn State University, Nokia Bell Labs, and IBM Research.

On Friday morning a panel session on "How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SiP," was chaired by the EPS president and Lyte. The discussion focused on the tools to achieve the goal, with panel members from University of Toronto, Lightmatter, University of Southern California, and substrate and PCB maker AT&S providing the discussion.

Options and challenges with large packages. Advanced packages for high-performance applications discussed at the conference included silicon interposers and fan-out on substrate using RDL, some with the use of an embedded bridge. Many of the presentations address the challenges with the large body size packages that are being driven by AI/ML where an increasing number of HBMs are required. TSMC described its progress with silicon interposers using its CoWoS process and the shift to an organic interposer instead of silicon with CoWoS-R and CoWoS-L. MediaTek reported on the challenges that it had to overcome with the solder mask cracking in large packages using fan-out RDLs. DNP described its 2µm line and space RDL structure and indicated that the use of the RDL instead of silicon interposer provides an improvement in resistance. ASE and Amkor presented papers describing their RDL structures with bridges. ASE explained co-design of a chiplet package with its FOCoS package versus a conventional FC-BGA. Amkor described its S-Connect bridge technology. IBM Systems described its AI hardware package using a high-density organic interposer.

Photonics/co-packaged optics. Co-packaged optics continues to be a hot topic with continued technical improvements. Rain Tree Photonics described its heterogeneously integrated wafer-level processed co-packaged optical engine for hyper-scale data centers. Broadcom discussed high-density integration

technologies for silicon photonics-based optical I/Os. Fraunhofer discussed photonic system integration with glass substrates. AIM Photonics with Analog Photonics demonstrated a 300mm Si photonics interposer. Siliconware (SPIL) described co-packaged optics on glass substrates for 1.2.4 Tb/s data center switches and fan-out bridge structures for co-package optics. Cisco described its low-cost, high-volume singulation of silicon photonic ICs for low-loss waveguide-to-fiber array edge coupling.

Photonics developments for LiDAR in autonomous driving were also presented. CEA-Leti and Steerlight described an advanced 3-D integration TSV and flip chip technology for mobile LiDAR.

New materials and processes. New materials and process developments provided insight into future packaging possibilities. Ajinomoto described its work in build-up film. Toray Industries provided details of its photodefinable low-Dk and low-Df polyimide for high-frequency applications. Resonac discussed its low-Dk/Df photoimageable dielectric for RDL. Taiyo Ink discussed a low-Df thermosetting film. AGC presented its work on a low-Dk build-up material using micron-sized hollow silica. NAMICS discussed its liquid compression mold underfill with low warpage and narrow gap flow. Deca Technologies and Nepes described maskless laser direct imaging and adaptive patterning for ultra-high-density fan-out packaging.

Mobile device packaging. Packaging for mobile devices also featured new developments. Samsung discussed its panel FO process for high-end mobile applications. SPIL presented a comparable study of RDL first versus last in a fan-out package-on-package (PoP).

Presentations from IBM/Fujikura, ASE, Renesas, Corning, Amkor/Texas Instruments, and several universities provided the latest developments in RF including antenna-in-package (AiP).

Don't forget about wire bonding, but watch the emerging technologies! Wire bonding still represents a large percentage of all packages and presentations from Onsemi described developments on modeling and optimization for Cu wire bonding. A special section was devoted to sintering and soldering for high-power, high-reliability, and RF devices. New material developments were provided by Indium and Uyemura. Pac Tech described its laser solder-jetting process. Samsung examined the risks of hybrid low-temperature solder on SMT and board-level reliability for BGA packages. GE Research discussed planar SiC power module packaging and interconnections using direct ink writing. Presentations also covered emerging areas such as additive manufacturing and packaging for flexible electronics.

Next year, ECTC will be held in Denver, CO.

E. JAN VARDAMAN is president of TechSearch International (techsearchinc.com); jan@techsearchinc.com.

https://www.pcdandf.com/pcdesign/index.php/current-issue/234-forefront/17373-advanced-packaging-the-hot-topic-in-the-florida-sun