

# IFTLE 561: Hybrid Bonding (HB) Update from Besi and EV Group – July 3, 2023

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#### Blogs, Packaging IFTLE

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Sorry for the disruption of the chronological flow of my recent blogs, but before I move on to the July coverage of the much-anticipated IMAPS "ONSHORING" conference, I wanted to continue covering a few of the papers from the 2023 IMAPS Device Packaging Workshop, which took place in March. As longtime readers of IFTLE know, we have been tracking the commercialization of "hybrid bonding" since it was first discussed and patented by Paul Enquist and his colleagues at Ziptronix in the early 2000s. It has emerged more than two decades later (Yes truly new technologies sometimes take a decade or more to catch on) as a key technology in high-density packaging such as 3D IC. Hybrid bonding (HB) involves simultaneous metal and dielectric bonding. It provides both mechanical support and dense electrical interconnects between vertically bonded chips. Cu is the commonly used interconnect. It has been the driving force for the miniaturization of CMOS image sensors and is currently being evaluated in 3D memory stacking including 3D NAND and SRAM. All the major packaging players such as TSMC, Intel, and Samsung have it on their process technology roadmaps (Figure 1).



#### Figure 1: Hybrid bonding (HB) process steps. (Source: Besi)

By the way, I've said it before and will continue to say, "It's about time that one of the major packaging societies like IEEE EPS and/or IMAPS gave Enquist and his Ziptronix team (now Adeia) one of their technical achievement awards. I think having your technology show up on Intel, Samsung, and TSMC roadmaps is justification enough...Don't you??

Anyway, its now common knowledge that "hybrid bonding" (HB) is becoming an integral part of our advanced packaging toolbox.

#### Besi and HB

The BESI presentation "*Chip-to-Wafer Hybrid Bonding Development for High Volume Manufacturing*" focused on BESI and Applied Materials (AMAT) declaration that hybrid bonding is the next-generation bonding technology (Figure 2).

	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Architecture			Heat compression force	Com	Car Distinguist Car Instanton Provide both
Contact Type	Wire	Solder ball or copper pillar	Copper pillar	RDL or copper pillar	Copper to copper
Contact Density	5-10/mm²	25-400/mm²	156-625/mm²	500+/mm <sup>2</sup>	10K-1MM/mm <sup>2</sup>
Substrate	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Accuracy	20-10µm	10-5µm	5-1µm	5-1µm	0.5-0.1µm
Besi & Applied Materials External					

# Figure 2: Timeline of interconnect process technologies. (Source: Besi)

The rest of the presentation addressed HB challenges, and BESI / AMAT proposed solutions.

- **CMP dishing**: Ensure proper thin barrier thickness and that barrier height is lower than SiOx profile.
- **Cleanliness:** Any particle on the bonding surface can lead to poor adhesion, weak bonding, or complete bond failure. This is a challenge for diced wafers on flex tape since the dicing process can introduce part
- **Plasma activation**: Bonding degrades with excessive time between activation and bonding. Also, when the plasma ion energy is too high the surface is roughened creating voids, which degrades the bonding.

The Chameo 8800 is Besi'schip to wafer bonder. They claim it is the first high volume die to wafer hybrid bonder (in production since 2022). They also claim it has 200µm placement accuracy (with 100µm in development and a roadmap to 50µm). It can place 2000 chips per hour and is designed for die pick up from a film frame / So/glass carrier.



# **Are You Listening?**



# EV Group and HB

The EVG presentation focused on "*D2W Hybrid Bonding using High Accuracy Carrier Solutions for 3D System Integration*" First EVG compared W2W and D2W HB (Figure 3).

	Hybrid W2W Bonding	Hybrid D2W Bonding	
Maturity	Wafer Bonding Equipment and Process are matured since 2010	Process and Equipment maturity is starting to yield but still many difficulties	
Contact Pitch	<1µm pitch in enabled in production	Currently 9µm pitch in production	
Die Size	Die Size and Grid Matching required	No limitations in die size and system segmentation	
Segmentation	Each bonding layer consist of one node	Each chiplet can consist of a different node	
Yield	Cummulative yield of each bonded layer	Cummulative yield can be avoided by testing	
Throughput	>25 bonds per hour possible	Related to chip size and amount of chiplets per system	

# Figure 3: Comparison of W2W and D2W HB (Source: Besi)

Figure 4 shows EVG's recently announced die-transfer technologies.

	Co-D2W	DP-D2W	SA-D2W
Transfer Method	Collective Die Transfer by Reconstituted Carrier	Direct placement of activated dies using Flip Chip Bonder	Self Assembly on hydrophilic guiding pads
Maturity	Limited volume production proven for several years	Feasibility testing ongoing	Experimental results available, Feasibility testing required

Figure 4: Comparison and readiness of die transfer technologies for HB. (Source: EV Group) EVG assessment of these options is shown in Figure 5:

	Co-D2W	DP-D2W	SA-D2W
Transfer Method	Collective Die Transfer by Reconstituted Carrier	Direct placement of activated dies using Flip Chip Bonder	Self Assembly on hydrophilic guiding pads
Pro's	<ul> <li>Proven technology</li> <li>Die Activation and cleaning equivalent to W2W hybrid bonding</li> <li>Oxide management</li> <li>Rework on carrier feasible</li> </ul>	<ul> <li>Versatile method</li> <li>Die thickness invariant</li> </ul>	<ul> <li>Avoids high precision flip chip bonder and potential cost saving</li> <li>Die thickness invariant</li> </ul>
Con's	<ul> <li>Error propagation of D2W + W2W alignment</li> <li>Cost of carrier prep, utilization and clean</li> <li>Die thickness needs to be in narrow range</li> </ul>	<ul> <li>Bonding interface needs to be touched</li> <li>Die handling especially for multi die stacks such as SRAM, DRAM</li> <li>Particle management during die placement</li> </ul>	<ul> <li>High precision die preparation using chemical treated zones</li> <li>Dicing potentially affects placement</li> <li>Die strain is affecting self alignment results</li> </ul>
Maturity	Limited volume production proven for several years	Feasibility testing required and ongoing	Experimental results available, Feasibility testing ongoing

Figure 5: Pros, cons, and maturity of die transfer methods for HB. (Source: EV Group) For all the latest on advanced packaging stay linked to IFTLE.....

For more on Hybrid Bonding, listen to the latest episode of the <u>3D InCites Podcast.</u>

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