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**Hybrid Bonding Moves Into The Fast Lane – July 21, 2022**

*Companies are speeding ahead to identify the most production-worthy processes for 3D chip stacking.*

The industry's unquenchable thirst for I/O density and faster connections between chips, particularly logic and cache memory, is transforming system designs to include 3D architectures, and hybrid bonding has become an essential component in that equation.

Hybrid bonding involves die-to-wafer or wafer-to-wafer connection of copper pads that carry power and signals and the surrounding dielectric, delivering up to 1,000X more connections than copper microbumps. It drives signal delay to negligible levels while accelerating bump density by three orders of magnitude over 2.5D integration schemes (see figures 1 and 2). While currently restricted to select high-end applications like HBM and processor/cache, hybrid bonding is set to rapidly proliferate to 3D DRAM, RF modems, and GaN/Si bonding for microLEDs.

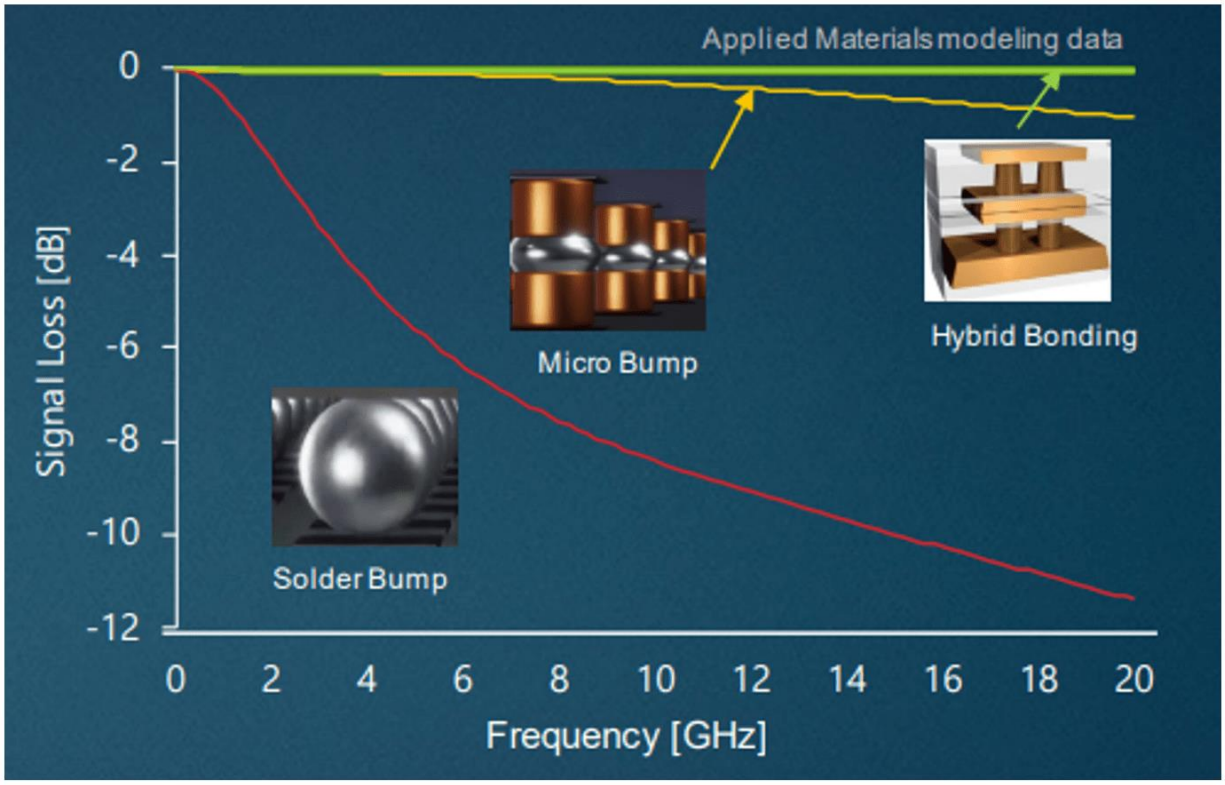


**Fig. 1: Hybrid bonding virtually eliminates signal loss. Source: Applied Materials**

But many process options are competing to play a part in this critical 3D arena. "It's not an exaggeration to say that hybrid bonding represents a turning point for the whole industry because it changes the way we are building devices," said Thomas Uhrmann, business development director at EV Group (EVG).

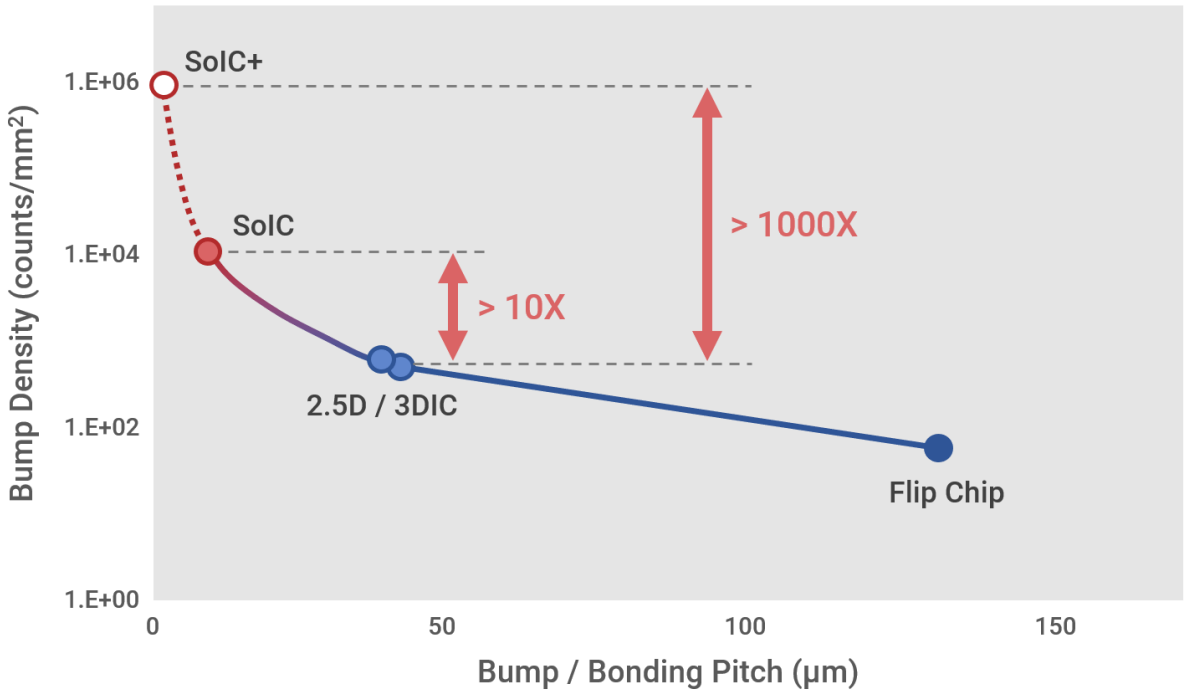


**Fig. 2: Bump density roadmap for SoIC and SoIC+. Source: TSMC**

Perhaps most impressively, hybrid bonding offers a viable alternative to transistor node scaling at a time when performance and power improvements are needed most.

For example, AMD's Ryzen 7-5800X3D processor, fabricated using TSMC's SoIC (System on Integrated Chip) process at 7nm, delivered a 15% performance increase and 3X power reduction without needing to fabricate the chips at 5nm. "AMD reported they could achieve the equivalent of a process node in performance using hybrid bonding. That is huge," said Laura Mirkarimi, vice president of semiconductor 3D at Adeia, an Xperi company. Adeia licenses IP of updated processes based on the first room-temperature hybrid-bonding process pioneered by Ziptronix in the early 2000s.

Intel, TSMC, and Samsung all provided the heads-up that copper bumps with solder tips would run into reliability problems when approaching 10µm dimensions — causing a shift to hybrid bonding. But even with hybrid bonding, tight control is required. "When we think about AR/VR, for example, you want to take RGB pixels and gallium nitride and attach those to a backplane. You can do it wafer-to-wafer, but there's a lot of burden on getting RGB into a single GaN, you can actually simulate and reconstitute what is probably on 200mm wafer into 300mm wafer for a good throughput. You have to be able to control what you're doing with the backplane as well as what you're doing with the individual pixels on the surface. So you have to start with the end requirement, and that can be a function of how much tolerance I have. Silicon photonics is a great example. The wave guides need a much higher level of control of the silicon nitride film than otherwise would be considered perfectly reasonable for different applications," said Gregg Bartlett, senior vice president of technology, engineering and quality at GlobalFoundries.

The bonding process itself can be room temperature, as in the Adeia process, or at higher temperature, as is the case in fusion bonding, which joins dielectric materials but not metals. Fusion bonding uses an epoxy glue layer and is being developed for backside power distribution schemes and for DDR6+ and next-generation memory devices (see figure 3 for applications). However, hybrid bonding always joins

both metal and dielectric films with no intermediate film. Imec demonstrated state-of-the-art hybrid bonding at IEDM last year with 700nm pitch copper hybrid bonding (see figure 3).[1]

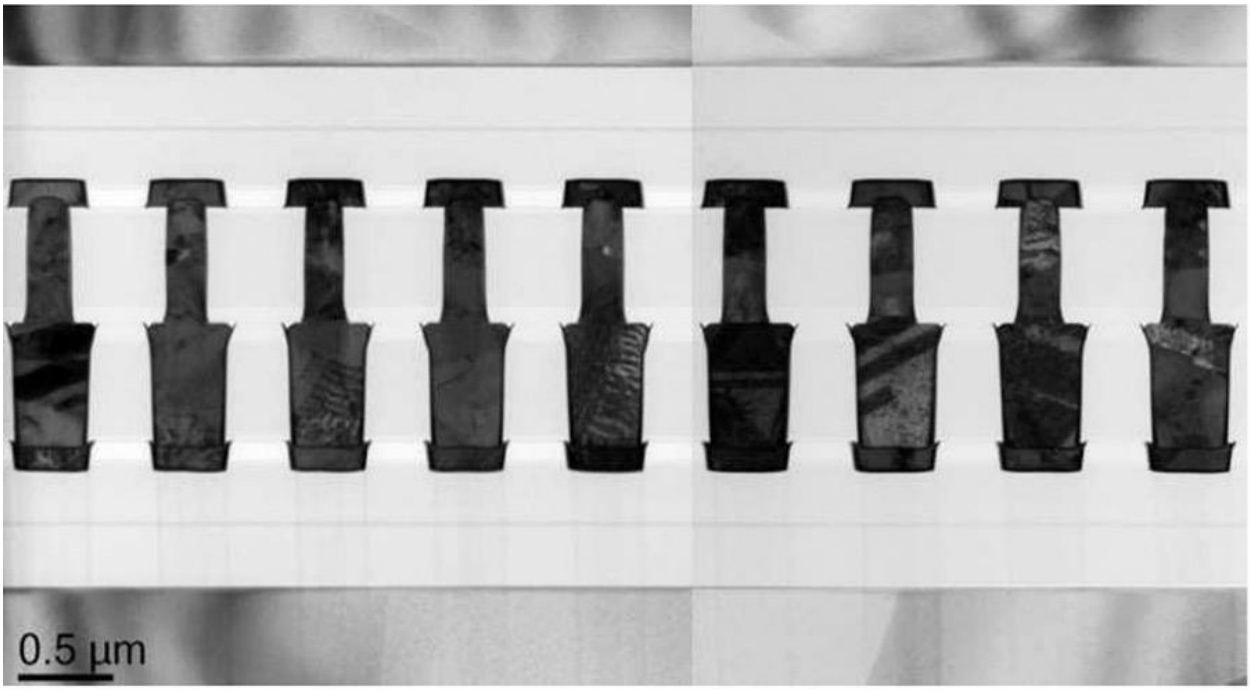


**Fig. 3: Wafer-to-wafer hybrid bonding with 700nm metal pitch. Source: Imec, IEDM**

**How it works**
Hybrid bonding's key process steps include electroplating (electrochemical deposition, ECD), CMP, plasma activation, alignment, bonding, singulation, and annealing. And though these tools are mature, for instance, for fabricating dual-damascene copper interconnects and flip-chip bonding, the processes need to be perfected for hybrid bonding's needs. These include <100nm alignment accuracy, new levels of cleanliness in chip-to-wafer bonding and singulation tools, exceptional CMP planarity with 0.5nm RMS roughness, and plating for optimal bonding.

"People are talking a lot about nanotwinned copper, but you're putting the copper in a more reactive state when you bond, so it diffuses fast," said Uhrmann. "At the end of the day, having good electrical conductivity and getting to a more electrodynamically stable orientation is the goal."

**It takes an ecosystem**
Several joint ventures and licensing agreements have formed to advance hybrid bonding, including:

- Adeia has licensing agreements with Micron, OmniVision, Skywater, SK Hynix, Sony, UMC, YMTC, etc.
- Applied Materials' dielectric dep, etch, CMP, plasma activation combines with Besi die bonder at Applied's Advanced Technology Development Center in Singapore
- EVG's fusion and hybrid bonding and collective assembly/metrology combines with ASM Pacific's 0.2µm die bonder at EVG's Heterogeneous Competence Center in Austria
- Intel and Leti developed a self-assembly process for die-to-wafer bonding using water evaporation
- Suss Microtec is combining its surface preparation overlay metrology tools with SET's die-to-wafer bonder

- TEL and IBM developed a 300mm module with silicon carrier wafer and laser release of thin product wafer

TEL and IBM Research's new 300mm module uses a silicon carrier wafer and an infrared laser to separate the thin silicon device wafer from a silicon carrier wafer, replacing a traditional glass carrier wafer. The companies noted that glass wafers are typically separated from thin silicon wafers by mechanical means, which introduces contaminants. Fabrication advantages of the silicon carrier approach include better tooling compatibility, fewer chucking issues, and fewer defects. In-line testing of thin wafers is also simpler. Additionally, TEL has an installed base of wafer-to-wafer fusion and hybrid bonding tools, plasma processing, and a range of wafer cleaning systems.

**A process evolves**

Wafer-to-wafer (W2W) hybrid bonding, which involves stacking the wafers face-to-face, bonding, annealing, and then singulating the stack, has a proven track record of success that began when Sony first used hybrid bonding for CMOS image sensors over a decade ago. "Hybrid bonding is in production for some companies using wafer-to-wafer, but die-to-wafer is much less mature and different approaches are being evaluated," said Kim Yess, executive director for WLP Materials at Brewer Science.

The wafer-to-wafer process begins with the wafer processed to the final BEOL interconnect level. A suitable dielectric is deposited (SiON, SiCN or $SiO_2$), which is then etched to create vias to the metal below. Barrier and seed layer are deposited, followed by copper plating. Copper pads are typically square. Copper CMP then polishes the overburden to provide slight dishing (several nm) below the planar feature. That miniscule gap will be filled when the copper expands upon anneal. Next, wafer cleaning removes all contaminants. Then a plasma activation step creates active sites on the dielectric. The two wafers are aligned precisely as they are brought together in the bonder and the sites form bonds. In the anneal oven, the copper fuses together, making electrical contact. Finally, wafer edge trimming is followed by backside wafer grinding to thin the wafer, cleaning and CMP polishing, etc. Voids in the bonded wafers are checked using surface acoustic microscopy (SAM). Voids will show up as white areas, whereas a void-free bond results in a black SAM image. (Figure 4 breaks down some of bonding mechanisms.)

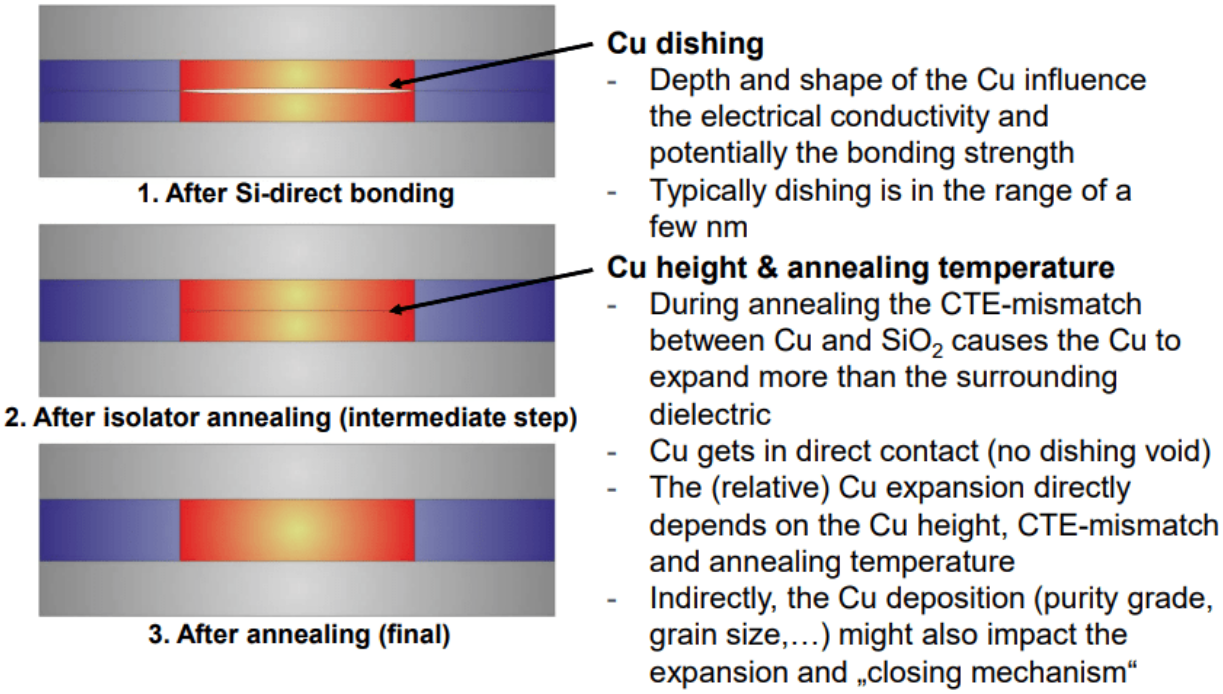

**Fig. 4: Control of physical properties throughout bonding. Source: EVG**

Two of the greatest concerns in hybrid bonding are process cleanliness and alignment accuracy. “For die-to-wafer what is important is to have the wafer surface really clean, to have absolutely no particles and no organic contamination. So the tool, which will put the dies on the wafer, needs to be absolutely clean, and every movement needs to be controlled,” said Emilie Bourjot, 3D integration project manager at CEA Leti. Specification is for <50 particles 90nm in size on a 300mm wafer.

Others agree. “The wafer surface — not just the copper, but the dielectric, as well — have to be pristine when you move to the bonding. Any foreign agents or contaminants of any kind, any imperfection or surface finish is going to end up impacting yield between those two wafers,” said John Ghekiere, vice president for product and technology at ClassOne Technology.

Copper plating is being optimized specifically for hybrid bonding. “The foundational requirements are the obvious ones, to fill features with copper with no voids. Then, the overburden layer needs to be extremely uniform because that’s what CMP is going to use to go do its job. So you need a nice uniform starting point,” said Ghekiere.

Together with Fraunhofer Institute for Electro Nano Systems, ClassOne is optimizing plating and hybrid bonding for microLED manufacturing. “Crystallographic structure is at the top of the list,” Ghekiere said. “The nice thing is that a lot of that tuning has already been enabled through partnership between the chemistry manufacturer and the tool vendor, where the chemistry is formulated to enable a certain grain orientation.”

Lam Research offers nano-twinned copper, fine-grained copper, and standard BEOL processes on its plating deposition platforms. Interestingly, the selection of copper type not only affects the copper properties, but also influences how high the anneal temperature needs to be to achieve good bonding. A recent study by Xperi (now Adeia) and Fraunhofer Institute for Reliability and Micro-Integration (IZM-ASSID) compared standard BEOL electroplated copper, nanotwinned copper and fine grain copper deposited on a Lam Sabre 3D system using a 10µm pad test vehicle with 40µm pitch.[2]

The copper was polished to the required profile needed for hybrid bonding. After room temperature bonding, annealing at various times and temperatures revealed that the nanotwinned and fine-grain copper films can lower the thermal budget by 20°C and 30°C, respectively. “So 20 or 30 degrees may not seem like a lot. But in reality, if you want to bring the thermal budget down to 175°C, which a lot of memory manufacturers are targeting, you can get there by moving to a different type of copper microstructure,” said Mirkarimi.

After plating, CMP planarity is critical. Requirements are on the order of less than few nanometers of variation, according to Woo Young Han, application engineering manager at Onto Innovation. Following CMP and cleaning, the surface is activated using a plasma process. A critical metric, according to Applied Materials, is the lag time between plasma activation and bonding.

“Any delay between activation and bonding can weaken the integrity of the bonds. Our integrated solution keeps contaminants away from the delicate surfaces,” said Sundar Ramamurthy, group vice president, Semiconductor Products Group at Applied Materials. He noted that robotics, software, and automation help to optimize process sequences to minimize the time between activation and bonding.

There are three options for singulating the dies — standard saw dicing, stealth (laser) dicing, and plasma dicing in a vacuum chamber. Standard dicing creates the most particulate matter. Stealth dicing and plasma etching in a vacuum chamber are much cleaner processes, but they come with higher cost-of-ownership than saw dicing. For hybrid bonding, the necessary level of cleanliness must be carefully weighed against the drive to lower processing cost.

**Collective bonding speeds throughput**

One the key advantages to collective alignment schemes is the ability to test and use known good die, according to Bourjot. Leti and Intel recently announced results from a collective die-to-wafer self-assembly process that uses the capillary forces of water droplets to align dies on a target wafer.[3] Developed over at least the last decade, Bourjot said the process (see figure 5) speeds alignment while achieving unprecedented accuracy. Through careful engineering of hydrophobic and hydrophilic interfaces, water drops are deposited on the wafer using a micropipette, and the batch of die are attached, giving initial rough alignment (>200µm). Then the water is evaporated, which itself performs the fine alignment (<400nm), and direct bond by van der Waals forces occurs at room temperature. Top and bottom overlay-like marks are used to characterize the alignment. Upon annealing, the van der Waals bonds convert to covalent bonds.

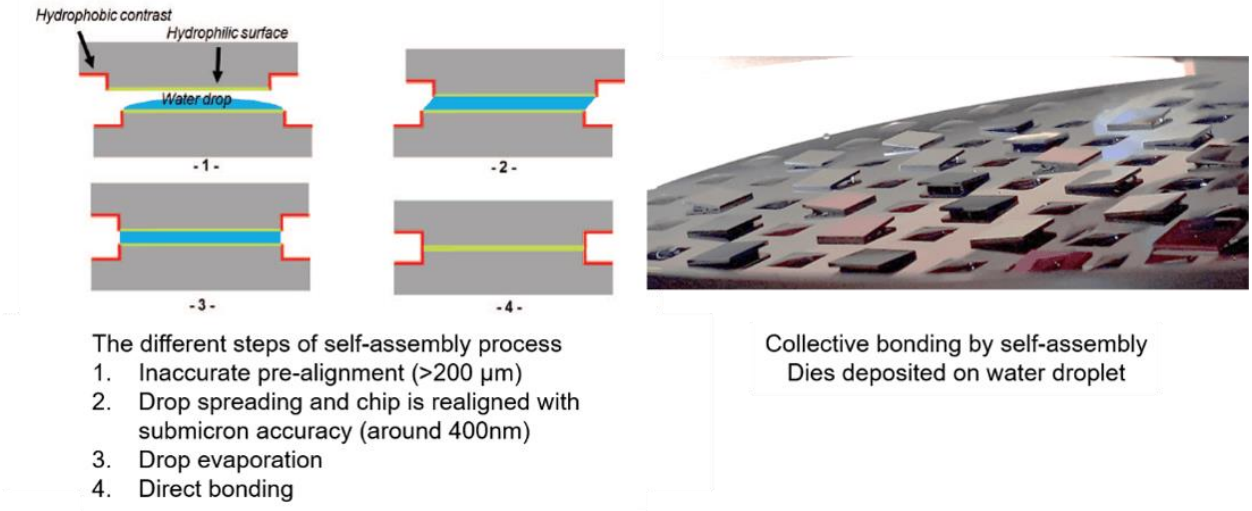


**Fig. 5: Collective self-assembly uses water droplets to self-align dies at room temperature followed by annealing. Source: CEA Leti**

In collective alignment, all die on the wafer are aligned simultaneously, rather than individually, which slows the process to the speed of the flip-chip tool — 1,000 dies/hour with placement accuracy of 1µm.

“In this case, our test vehicle is 40 dies, but you can imagine many more dies on the holder. All of the dies are bonded simultaneously, so the limiting point here is the time to populate the holder,” said Bourjot.

She estimates commercial throughput to be in the 10,000 die/wafer range. In describing the researchers’ laboratory collective self-assembly bonding tool, she said, “The low-reproducibility, manual process control nonetheless achieved alignment of 500nm and below, which strongly suggests that an industrial tool dedicated to this process would deliver higher reproducibility, robustness and precision.” The researchers seek an industrial partner for tool development and process refinement.

“Collective die-to-wafer approaches are the most universal because you’re decoupling the assembly from the bonding and you can protect the dies during the placement,” said EVG’s Uhrmann. “So you protect the wafer surface from all the mechanical gripping and touching that is going on in the flip-chip bonder.”

**Metrology and test**

Metrology systems for hybrid bonding require high sensitivity while accommodating whole wafers, diced wafers on film frames, and reconstituted wafers on carriers. KLA’s Kronos 1190 inspection system combines a darkfield channel for small particle detection and brightfield channel for detecting residue defects.

Alignment is checked using overlay marks. “Different devices have different needs in 3D integration in terms of metrology. For some, it might be okay to check overlay before bonding and after bonding. But for a lot of devices, you will need to have an electrical test pre- and post-bonding, so it’s not making things easy,” said Uhrmann.

**Conclusion**

Hybrid bonding processes are rapidly maturing to meet incredible demand from high-end processors, HBM, microLED, and other markets. Collaborative approaches are key to resolving the many contamination, process integration, and thermal budget constraints associated with making this technology accessible beyond just high-end device manufacturers. Importantly, hybrid bonding is bringing front-end and back-end processes together, along with opportunities for partnerships that bridge this gap.

**References**

1. E. Beyne, et. al., “3D SoC Integration, Beyond 2.5D Chiplets,” IEDM 2021.
2. L. Mirkarimi, et.al., “The Influence of Cu Microstructure on Thermal Budget in Hybrid Bonding,” IEEE ECTC, May 2022.
3. A. Bond, et.al., “Collective Die-to-Wafer Self-assembly for High Alignment Accuracy and High Throughput 3D Integration,” IEEE Electronic Components and Technology Conference, May 2022.

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