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As Chiplets Go Mainstream, Chip Industry Players Collaborate to Overcome New Development Challenges – February 16, 2023

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Key issues in establishing a multi-vendor chiplet ecosystem.

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The semiconductor industry is building a comprehensive chiplet ecosystem to seize on the advantages of the devices over traditional monolithic system-on-chips (SoCs) such as improved performance, lower power consumption, and greater design flexibility. With heterogeneous integration (HI) presenting significant challenges, collaboration to fulfill the potential of chiplets has become even more important. Industry experts gathered at the Heterogeneous Integration Summit at SEMICON Taiwan 2022 to offer perspectives on how the growing chiplet ecosystem is working to overcome these headwinds.

“Looking at the big picture, the development of semiconductors is actually all about system integration being done efficiently,” said C.P. Hung, VP of Corporate R&D Center of ASE Group and Co-Chair of SEMICON Taiwan Packaging and Test Committee, speaking at the. “System integration can be divided into two types of HIs – homogeneous integration and heterogeneous integration. While going deep into HI technologies, we must continue to strengthen and facilitate the cooperation among members of the industry chain in order to overcome the various challenges that might arise along the way.”

Chiplets gain momentum

Jan Vardaman, President of TechSearch, a market research leader specializing in technology trends in microelectronics packaging and assembly, pointed out that IC designers find it easier and more flexible to make the chips they want with chiplets. Chiplets also reduce chipmaking costs by enabling the production of different functional circuits using the most cost-effective processes without necessarily having to rely on the most advanced technology.

With chiplets enabling greater flexibility and better cost structures possible, more chiplet-based devices have been launched in the markets. However, because they’re developed independently by different manufacturers, chiplet products are often not interoperable and compatible, resulting in a fragmented chiplet ecosystem. That is why the launch of UCIe standard, which seeks to break barriers, is an important milestone in the development of chiplets.

Executives from the following organizations presented at the Heterogeneous Integration Global Summit 2022. Left to right: Lewis Huang, Vice President of Senju Electronic (Taiwan); C.P. Hung, Vice President of ASE Group; Akshay Singh, Vice President of Advanced Packaging Technology Development, Micron; Shin-Puu Jeng, Director of APTS/NTM, TSMC; HW Kao, VP, Manufacturing Operations and Supply Chain Management of MediaTek; Albert Lan, Global Sr. Packaging Account TD Head of Applied Materials; Yu Po Wang, Vice President of CRD Center, Siliconware Precision Industries; Yu-Hua Chen, Vice President of Unimicron Technology; John Ostrowski, Managing Director of SABRE 3D, Lam Research; Damon Tsai, Senior Product Director of Inspection Business Unit, Onto Innovation.

Raja Swaminathan, Corporate Vice President of Advanced Packaging at AMD, believes market demand is one a key factor driving the semiconductor industry's transition to heterogeneous integration. The push for higher processor performance in the high-performance computing (HPC) market can no longer be met only by process scaling. As a processor supplier, AMD must find new ways to satisfy customers' needs, and chiplets are among the most effective solutions. Chiplets have allowed AMD to overcome cost and scaling challenges and launch products to better fulfill market demand.

"The key to further promoting the development of the chiplet ecosystem lies in how to transfer the research results of the industry to the educational system," said William Chen, Chair of HIR and Fellow at ASE Group. "Everything from design methods to technologies is in the hands of the industry as it focuses more on chiplets. Yet there's a shortage of students studying chiplet design in schools. We all know too well that talent matters to the development of semiconductors. Only by bringing chiplets to more students in schools can we see more chiplet-based technologies happening in the future."

LogoDon Chan, Vice President of R&D at Cadence, said chiplets have powered a paradigm shift in the world of IC design. By breaking SoC down various chip functions into chiplets and assembling them into a

single device through advanced packaging, IC designers have found a new path out of the Power-Performance-Area (PPA), the three major components of a process technology they've been trying to balance. This trend, nevertheless, presents new challenges, such as how to split the functions originally integrated in the SoC and design the chiplet interconnect architecture plets, and overcome heat dissipation challenges from chip stacking – among the hardest to solve. Design processes, methodologies and tools need to evolve to overcome these obstacles.

"For IC designers, the most interesting and valuable aspect of chiplets is that they turn IC design into mixing cocktails," said HW Kao, VP of Manufacturing Operations and Supply Chain Management at MediaTek. "One can create a unique product by mixing different materials. Die partitioning – dividing the functions desired by customers into multiple chips – has become the only way to go."

In practice, MediaTek finds that die partitioning helps reduce costs, and some functions can be made with more mature and more cost-effective manufacturing processes. The areas of individual chips are getting smaller, making better production yield possible.

Heat dissipation: great potential in immersion cooling

As chiplets made possible with advanced packaging are fueling an important tech wave in semiconductor manufacturing, device overheating – long a significant challenge – will only become more complicated with packaging advances.

Sunlai Chang, President of Wiwynn Corp, said the entire industry chain upstream to downstream will need to work together to improve heat dissipation in a more effective way. Wiwynn has been developing immersion cooling solutions in recent years since heat generated by chips can no longer be removed by fans alone liquid cooling technologies near their limits. Chang said immersing the entire motherboard together with the electronic components coolant will be the future of heat dissipation.

"The current packaging technology used in semiconductor devices has not been optimally designed for immersion cooling," said Chang, who is eager to collaborate with partners in the packaging industry to develop new solutions.

Attendees explore semiconductor advanced packaging technology opportunities at the Heterogeneous Integration Global Summit 2022.

CPO to become key to optimizing power consumption

With the I/O units responsible for data transmission also a significant heat source, the continuous improvement of computing performance and the increase of I/O bandwidth, reducing I/O power consumption will become more challenging, said Jie Xue, Vice President of Technology and Quality at Cisco Systems. “There’s no limit to the growing amount of internet data, and the I/O bandwidth requirements of Netcom chips are getting higher and higher. But the truth is that traditional transmission media can no longer carry such a large amount of data at an acceptable power consumption level. Netcom ASICs enabled by Co-package Optics (CPO) technologies such as silicon photonics are becoming the major trend.”

CPO is a typical HI that integrates logic units using CMOS process and photoelectric and optical components made with special process through advanced packaging technology, allowing chip developers to not only obtain more communication bandwidth, but also drastically reduce power consumption in data transmissions.

TSMC on the Latest CoWoS Solutions

TSMC, the world’s largest contract manufacturer of the semiconductor chips, shared the latest developments in its CoWoS technologies. Shin-Puu Jeng, Director of APTS/NTM at TSMC, said the company began developing CoWoS advanced packaging technology years ago to meet needs of HPC customers and today offers a CoWoS product family.

Jeng said TSMC's CoWoS customers have different requirements. While some value performance, other want high-density wires or greater cost-effectiveness. For example, CoWoS, which originally used a silicon interposer, was later upgraded to CoWoS-R, which replaced the silicon interposer with an organic interposer and has better response speed and energy consumption with low-impedance wire. The integration of the chip can rise to yet another level by assembling decoupling capacitor passive components, making CoWoS-R a perfect choice for high-power system integration.

Equipment and material players focus on hybrid bonding, launch various solutions

Key semiconductor industry companies including Applied Materials, Brewer Science, EVG, Lam Research, and SPI also presented at the Heterogeneous Integration Summit, discussing advanced packaging technologies used in chiplet integration, equipment, materials and their solutions.

Hybrid bonding was an especially hot topic at last year's event, with almost all advanced packaging players leveraging the process to shrink on-chip interconnections and bonding as much as possible to meet the extreme requirements of interconnection density in advanced packaging. And while it is possible to use hybrid bonding in mass production today, many technical issues still need to be addressed.

Developers of solutions to hybrid bonding technical challenges stand to benefit significantly from market opportunities. Solution and service providers across the various stages of the semiconductor manufacturing, from equipment and materials to test and measurement, have proposed new and intriguing solutions for processes incorporating hybrid bonding.

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