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Current And Future Packaging Trends – August 19, 2021

Experts at the Table: Rising costs and the physical limits of reticles is forcing more companies to examine alternatives to shrinking geometries.

Semiconductor Engineering sat down to discuss IC packaging technology trends and other topics with William Chen, a fellow at ASE; Michael Kelly, vice president of advanced packaging development and integration at Amkor; Richard Otte, president and CEO of Promex, the parent company of QP Technologies; Michael Liu, senior director of global technical marketing at JCET; and Thomas Uhrmann, director of business development at EV Group. What follows are excerpts of that conversation.

SE: IC packaging isn't new. Years ago, packaging more or less was in the background. A given IC package simply encapsulated and protected a chip. Recently, though, packaging has become more important across all industries. What changed?

Chen: Packaging used to be in the background, but times have changed. There are several reasons for that. Moore's Law is reaching either the beginning of the end, the middle of the end, or coming to the end. We are at the 5nm node, and 3nm and 2nm nodes are on the horizon. And then what? At these nodes, the die becomes very expensive. And we want to utilize the die as economically as possible. At the same time, the users or chip designers want to have chips with good yields. To have everything they want, the die will reach the reticle range. All of these things are coming together. So now we are saying, 'Why don't we break the die apart into smaller pieces?' There are some leading companies doing this, and they are doing it very effectively. That's called chiplets. In chiplets, we are dealing with multiple chiplets in a package. But when you have multiple chips interconnected in the package, you have to ask how do you package it electrically, thermally, and mechanically? So that explains one of the reasons why packaging is coming to the forefront.

Kelly: If you go back in time, packaging was always important. I like to think of things in ratios, or the ratio of performance to cost. Packaging has always participated in that ratio, but it has been dominated by the cost portion of the ratio. Recently, as you go into things like heterogeneous integration and chiplets, packaging is enabling the performance side of the ratio. Cost is still there. Everybody wants to have better performance at the lowest possible cost. Once again, packaging was always important, but now it's important in the performance side of that ratio. In some cases, it's enabling, whether it's transistor count or whether it's miniaturizing the size of the latest nodes, so you don't have to spend more than you need to get the full integration. Those are a couple of reasons that everyone's paying attention to packaging. It's directly related to product performance.

Otte: Moore's Law was really aimed at the semiconductor chip itself because it focused on making only the chip features smaller. Those benefits were so great that the industry never focused on packaging, meaning leadframes, circuit boards, and connectors. Thus, the rate of progress in electronic interconnects over the years has been a lot less. Today, in building smaller, higher-density electronic devices, we are to the point where 5 microns is about as fine as you can do with classic mechanical assembly. The semiconductor industry learned how to make things with high precision that are smaller than that. So all of a sudden we find ourselves utilizing the techniques we developed for making chips to fabricate packaging, and we are able to make things small enough. Technically, interconnects can be a lot smaller than most of them are. We have left them large so we can see and handle them. But now, the pressures for added functionality and greater heat dissipation are forcing us to get more functionality per unit volume for packaging, as well as the die, implying making the interconnects smaller.

SE: Let's look at the second half of this year or over the next year. From your vantage point, what are you seeing out there?

Liu: Before I pull out my crystal ball, let me add to the previous question. In addition to cost, performance, functional density, as well as the evolution of Moore's Law from the silicon level to the package level, a practical consideration for time to market is warranted. This is especially important for OSATs when evaluating the true business case of chiplets. It's indeed a huge consideration for OSATs, and an ultimate factor that determines whether, when, and how to invest in chiplets. Whenever our customers talk to us about chiplets, they always ask this question: 'How much will chiplets help us in terms of time to market?' We always find it very challenging to quantify an answer for them. The whole value chain of heterogeneous integration is not yet clear. That's something for all of us — OSATs, foundries and IDMs — to think about along the way. Meanwhile, looking at what's ahead, we foresee the chip shortage situation to continue, unfortunately, until the end of next year. That's a very rough prediction, and there are two reasons behind this. Number one, we just don't see a shortcut for the whole supply chain to fully catch up on the demand we have seen so far. From our perspective, we have seen a backlog of orders till the end of this year and early next year. That pretty much means full-capacity demand. Number two, we have been very strong in communications, mobile and 5G. On the high-performance computing and automotive side, we've also seen a huge spike when it comes to customer demand during the last few months. The aforementioned two indicators have also driven us to look into innovative ways to satisfy demand in the most efficient manner. As we've learned, bidding for new equipment alone doesn't offer a complete answer. OSATs have to be creative and smart about how to best utilize our existing capacity and resources in order to ride out this IC shortage wave, while getting prepared for an inexorable correction or even downturn.

Uhrmann: The big players are realizing the role of packaging. That shift has become more obvious over the last three years. One important step was the official announcement of a packaging roadmap by IDMs and foundries on the insertion point for the next nodes in packaging. There was the belief that the 10µm level was always the bump pitch limit for standard packaging. And below 10µm, the industry requires new interconnect technology. In this case, it's hybrid bonding. That insertion point of 9µm is pretty clear, and was made pretty clear by the major players. That tells us how they will proceed, and where the new nodes are driving the advanced packaging industry. Of course, if you're scaling a transistor, the package and the interconnect need to scale in the same way. That's what people are forgetting in the whole discussion. That's definitely one of the trends. In addition, the PPAC (power, performance, area, cost) ratio will continue to be one of the major drivers for why we need packaging. Scaling is becoming difficult. The reticles are getting very large, and the packages and systems on chips are getting more complex. One of the solutions here is smart packaging. This is increasing the importance of packaging. We have very expensive chips that we have to deal with and that we have to package. The first point of insertion here for a new packaging technology is high performance. We are not only seeing packaging for electronic systems, but also packaging of photonics. We will see more lidar and depth sensing, which requires different packages and processes. The same is true with sensors for automotive.

Kelly: The move toward heterogeneous and chiplets has been underway for a good long while. In addition, we've also seen these latest market trends like chip shortages and substrate shortages. That's just adding fuel to the discussion about how to economize on the latest silicon nodes, especially during the initial silicon node start, when wafers are in short supply. These trends in the marketplace with regard to material shortages is stimulating that discussion somewhat. Then, on the technology side, this trend toward heterogeneous integration requires an increase in the number of package-level signals to permit separate die-to-die communications, similar to a functional block to a functional block inside of an SoC. Once the IC packaging infrastructure is broadly available and the electrical/mechanical specifications for these common interfaces are adopted, then I expect the conversion to heterogeneous packages will accelerate. Silicon photonics is also going to benefit from these developments and will grow significantly in the next couple of years.

Chen: On the automotive side, we have two trends. One is the electrification trend. The other thing that people have said is we are going to have a smartphone on wheels. That is to say, we want to have a

significant amount of environmental sensing, vehicle-to-vehicle communication, and high-performance computing in the vehicle. However, this is presenting some tremendous challenges for packaging. We already have high-performance computing sitting in an air-conditioned room. Now, we are talking about high-performance computing sitting in the car. It's communicating with other cars, communicating with the cloud, and also communicating within itself. These present some important challenges for our industry. Many are packaging issues. The electronics for a server in a data center, or a smartphone in a consumer's hand have very different requirements to an autonomous automobile on the road. These are areas that are yet to be fully explored, but they are going to present great challenges for us. Smartphones and data centers have been key drivers for semiconductor innovation. And we now see automotive evolving at a significant pace. These applications all have their unique needs and requirements, but at the same time, they all help each other. Innovative packaging technologies are not limited to one application, but instead, they are cross-fertilizing and adding value across an increasing number of applications.

SE: Advanced packaging tends to grab the headlines and are making inroads. Yet, wire-bond and flip-chip are still widely used today. In fact, a large percentage of all packages use wirebonding. What's happening here?

Otte: Wirebond continues to be widely used because it's so easy to reconfigure. You don't have to go through a process of re-fabricating a substrate or die. You can just reprogram the wirebonder, which is about a 15-minute activity. So that's why wire bonding continues to be used. Given that versatility, people keep working to incrementally improve wire bonding. We are now using copper wire and silver plated copper wire. Those are all improvements on the margins. They are not factors of two. These are factors of 5% and 10% here and there, which in total turn out to be important. And as volumes grow, it's worthwhile doing all of that. I anticipate those kinds of changes continuing forever in our technologies, as things do what I'll call 'approach the asymptote' in almost anything we address. To me, though, the more difficult issues relate to these emerging technologies and how we incorporate them. For example, we have thermal compression bonding with 10,000-plus bumps and driving the pitch down. There's much benefit to reducing the pitch on these bumps, but that's one of the really hard things to do for a variety of reasons. There are the co-planarity issues. There are the contamination issues. There are building redundancy or making sure all 10,000 bumps connect, and those kinds of issues. When we have these large numbers, the statistics start to work against you. A failure of one bump in a million becomes an expensive phenomenon if you are bonding 10,000 bumps.

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